TC–10B

FREQUENCY-PROGRAMMABLE ON/OFF CARRIER TRANSMITTER/RECEIVER

System Manual

CC44–VER02

(Replaces CC44–VER01)

Pulsar
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Printed April 1997

TC–10B

System Manual
CC44–VER02

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Important Change Notification

This document supersedes both the *TC–10B Frequency-Programmable On/Off Carrier Transmittter/ Receiver System Manual CC44–VER01*, last printed in April 1996, and the *Addendum to CC44–VER01*, printed September 17, 1996. The following list shows the most recent publication date for each chapter. Publication dates in **bold type** indicate changes to that chapter since the publication of the *Addendum to CC44–VER01* printed September 17, 1996. For these chapters, the specific pages that have changed are listed for easy reference. Note that only significant changes, i.e., those changes which affect the technical use and understanding of the document and the TC–10B equipment, are reported. Changes in format, typographical corrections, minor word changes, etc. are not reported. Note also that in some cases text and graphics may have flowed to a different page than in the previous publication due to formatting or other changes. The page numbers below show the current pages on which the reported changes appear.

Each reported change is identified in the document by a change bar placed in the margin to its immediate left, just like the one on this page.

Chapter Number & Title	Publication Date	Pages with Changes
Front Section	**April 1997**	ii, vi, vii, x
1. Product Description	September 1996	
2. Applications and Ordering Information	**April 1997**	2-6 thru 2-21
3. Installation	**April 1997**	3-13
4. Test Equipment	January 1996	
5. Acceptance Tests	**April 1997**	5-3, 5-5, 5-8
6. Routine Adjustment Procedures	**April 1997**	6-7, 6-8, 6-11, 6-12, 6-13
7. Signal Path	**April 1997**	7-7
8. Maintenance	September 1996	
9. Power Supply Module	January 1996	
10. Keying Module	January 1996	
11. Transmitter Module	**April 1997**	11-7
12. 10W PA Module	January 1996	
13. RF Interface Module	January 1996	
14. Receiver/Synthesizer Module	April 1996	
15. Level Detector and CLI Module	January 1996	
16. Receiver (solid state) Output Module	**April 1997**	Entire Chapter
17. Automatic Checkback System	**April 1997**	17-1, 17-6, 17-12
18. Optional Voice Adapter Module	January 1996	

We recommend that you become acquainted with the information in this manual before energizing your TC–10B system. Failure to do so may result in injury to personnel or damage to the equipment, and may affect the equipment warranty. If you mount the carrier set in a cabinet, it must be bolted to the floor or otherwise secured before you swing out the equipment, to prevent the installation from tipping over.

You should not remove or insert printed circuit modules while the TC–10B is energized. Failure to observe this precaution can result in undesired tripping output and can cause component damage.

All integrated circuits used on the modules are sensitive to and can be damaged by the discharge of static electricity. You should observe electrostatic discharge precautions when handling modules or individual components.

PULSAR does not assume liability arising out of the application or use of any product or circuit described herein. PULSAR reserves the right to make changes to any products herein to improve reliability, function or design. Specifications and information herein are subject to change without notice. All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If you desire further information regarding a particular installation, operation, or maintenance of equipment, please contact your local Pulsar Technologies, Inc. representative.

PREFACE

Scope

This manual describes the functions and features of the TC–10B Power Line Carrier Transmitter/Receiver. It is intended primarily for use by engineers and technicians involved in the installation, alignment, operation, and maintenance of the TC–10B.

Equipment Identification

The TC–10B equipment is identified by the Catalog Number on the TC–10B chassis nameplate. You can decode the Catalog Number using the Catalog Number Table in Table 2-2 and Table 2-3 (see Chapter 2).

Production Changes

When engineering and production changes are made to the TC–10B equipment, a revision notation (Sub number) is reflected on the style number, related schematic diagram, and associated parts information. A summary of all Sub numbers for the particular release is shown on the following page.

Warranty

Our standard warranty extends for either 18 months after the equipment is in-service or 24 months after shipment, whichever comes first. For all repaired modules or advance replacements, the standard warranty is 90 days or the remaining warranty time, whichever is longer. Damage clearly caused by improper application, repair, or handling of the equipment will void the warranty.

Equipment Return & Repair Procedure

To return equipment for repair or replacement:

1. Call your PULSAR representative at **1–800–785–7274**.
2. Request an **RMA number** for proper authorization and credit.
3. Carefully pack the equipment you are returning.

   Repair work is done most satisfactorily at the factory. When returning any equipment, pack it in the original shipping containers if possible. Be sure to use anti-static material when packing the equipment. Any damage due to improperly packed items will be charged to the customer, even when under warranty.

   Pulsar Technologies, Inc. also makes available interchangeable parts to customers who are equipped to do repair work. When ordering parts (components, modules, etc.), always give the complete PULSAR style number(s).
4. Make sure you include your return address and the RMA number on the package.
5. Ship the package(s) to:

   Pulsar Technologies, Inc.
   Communications Division
   4050 NW 121st Avenue
   Coral Springs, FL 33065

Document Overview

The TC–10B circuitry is divided into eight (8) standard modules. In addition, Automatic Checkback and Voice Adapter modules are available as options. (See Chapter 7, Figure 7-1, for a Functional Block Diagram.)

Chapter 1 provides the Product Description, which includes specifications; module circuit descriptions and troubleshooting procedures are in Chapters 9 thru 18. Chapter 2 presents applications and related catalog numbers for ordering purposes. The TC–10B installation is described in Chapter 3, with maintenance procedures in Chapter 8. Chapters 4, 5, and 6 identify test equipment, acceptance tests, and adjustment procedures, respectively, while Chapter 7 describes the TC–10B signal path (for use during testing).

Contents of Carrier Set

The TC–10B carrier set includes the style numbers, listed below, with appropriate sub numbers representing revision levels. (To determine related style numbers, you may also refer to Table 2-3.)

Module	Style	Sub Number
Power Supply	1617C38 GXX	2
Keying	1606C29 G01	7
Transmitter	1610C01 G01	8
10W PA	1606C33 GXX	20
RF Interface	1609C32 GXX	8
Receiver	1606C32 GXX	21
Synthesizer	1585C56 GXX	20
Level Detector and CLI	1606C34 GXX	7
Receiver Output	CC20-RXSMN-001	1
Automatic Checkback (Master)	1606C37 G01	16
Automatic Checkback (Remote)	1606C38 G01	8
Voice Adapter	1606C39 G01	16

FIGURES

FIGURES, Cont'd

FIGURES, Cont'd

TABLES

TABLES, Cont'd

Chapter 1. Product Description

1.1 Standard Features

The TC–10B frequency-programmable power-line-carrier set offers the following features as standard:

- Programmable over 30–535 kHz (in 0.5 kHz steps) with direct frequency readout
- Frequencies are easily field-selectable by rotary switches
- Wideband (1,200 Hz) receiver for use with all blocking systems
- Narrowband (600 Hz) receiver for use with directional-comparison blocking systems where there is a need to improve signal-to-noise ratio (SNR)
- High receiver sensitivity: 60 mVrms....Wideband
20 mVrms....Narrowband
- Universal keying/receiver output
- 300-2,000 Hz range audio channel for maintenance Voice Channel
- Built-in low/high level carrier test switches
- dc-to-dc isolated power supply
- 48, 125, and 250 Vdc versions available

1.2 Standard Nomenclature

The standard nomenclature for PULSAR carrier protection equipment is as follows:

Cabinet – contains fixed-racks, swing-racks, or open racks

Rack – contains one or more chassis (e.g., the TC–10B)

Chassis – contains several printed circuit boards, called modules (e.g., Transmitter or Receiver)

Module – contains a number of functional circuits (e.g., Oscillator or Synthesizer)

Circuit – a complete function on a printed circuit board

1.3 TC–10B Chassis

The TC–10B chassis specifications include standard dimensions of:

Height – 5.25” (133.35 mm), requiring 3 rack units, each measuring 1.75” (44.45 mm)

Width – 19.00” (482.6 mm) **Depth –** 13.50” (342.9 mm)

Each chassis is notched for mounting in a standard relay rack.

1.4 TC–10B Modules

The TC–10B circuitry is divided into standard modules with optional Voice Adapter and Automatic Checkback modules available, as shown on the Functional Block Diagram (Chapter 7). Circuit descriptions, complete with schematic diagrams and parts lists for each module, are shown in Chapters 9 through 18 with Sub Numbers that indicate appropriate revisions for each module, as follows:

Chapter	Module	Schematic	Parts Lists
9.	Power Supply	1617C38-2	1617C38-2
10.	Keying	1606C29-7	1606C29-7
11.	Transmitter	1355D71-8	1610C01-11
12.	10W PA	1606C33-20	1606C33-20
13.	RF Interface	1609C32-8	1609C32-8
14.	Receiver	1606C32-21	1606C32-21
	Synthesizer	1585C56-20	1585C56-20
15.	Level Detector and CLI	1606C34-7	1606C34-7
16.	Receiver Output (Solid State)	CC20-RXSMN-001	CC40-RXSMN
17.	(Optional) Automatic Checkback System, Master	1606C37-16	1606C37-16
17.	(Optional) Automatic Checkback System, Remote	1606C38-8	1606C38-8
18.	(Optional) Voice Adapter	1606C39-16	1606C39-16

NOTE

See Chapter 2, Applications and Ordering Information, for ordering information. See Chapter 3, Installation, for a summary of jumper controls.

1.5 SPECIFICATIONS

The TC–10B meets or exceeds all applicable ANSI/IEEE standards.

1.5.1 Transmitter/Receiver

Table 1-1 lists the Transmitter/Receiver specifications for the TC–10B.

Table 1–1. Transmitter/Receiver Specifications.

Frequency Range	30–535 kHz in 0.5 kHz (500 Hz) steps, transmitter selection in 100 Hz steps
4-Wire Receiver Input Impedance	5,000 ohms or 1,000 ohms
RF Output Impedance	50, 75 or 100 ohms (nominal unbalanced)
Output Power	• 10 watts (max) • 100 watts (with optional external amplifier)
Frequency Stability	± 10 Hz (typical)
Nominal Receiver Bandwidths	• Wideband: 1,200 Hz at 3 dB points • Narrowband: 600 Hz at 3 dB points
Minimum Receiver Bandwidths	• Wideband: 1,020 Hz at 3 dB points • Narrowband: 520 Hz at 3 dB points
Harmonic Distortion	55 dB below full power

Receive Sensitivity		
Wideband	• (5,000 ohms) • (1,000 ohms)	60 mVrms (min), 70 Vrms (max) 15 mVrms (min), 17 Vrms (max)
Narrowband	• (5,000 ohms) • (1,000 ohms)	20 mVrms (min), 70 Vrms (max) 5 mVrms (min), 17 Vrms (max)
(See Figure 14-4 in Chapter 14 for selectivity characteristics.)		

Table 1–1. System Specifications (Cont'd).

Minimum Channel Spacing	
Wideband	4 kHz
Narrowband	2 kHz
With Voice Adapter (both Narrowband and Wideband)	4 kHz
An external hybrid or other device offering at least 20 dB rejection of the adjacent channel must be used in the application	

Channel Speed at 15 dB Margin, Solid State Output	
Wideband	2.5 ms (pickup) 2.5 ms (dropout) typical
Narrowband	3.6 ms (pickup) 3.6 ms (dropout) typical
Channel Time for Wideband Phase-Comparison	2.0 ms ... typical

1.5.2 Keying

Table 1-2 shows the TC–10B keying specifications.

Table 1–2. Keying Specifications.

Carrier Start, Carrier Stop Auxiliary (Reduced Power) Keying	All optically isolated for operation at 15 V, 48 V, 125 V, or 250 Vdc, strappable for either presence or absence of voltage for keying, as well as carrier start or stop priority (maximum burden is 20 mA).
Manual Keying	Recessed pushbutton switches for carrier start and auxiliary keying.

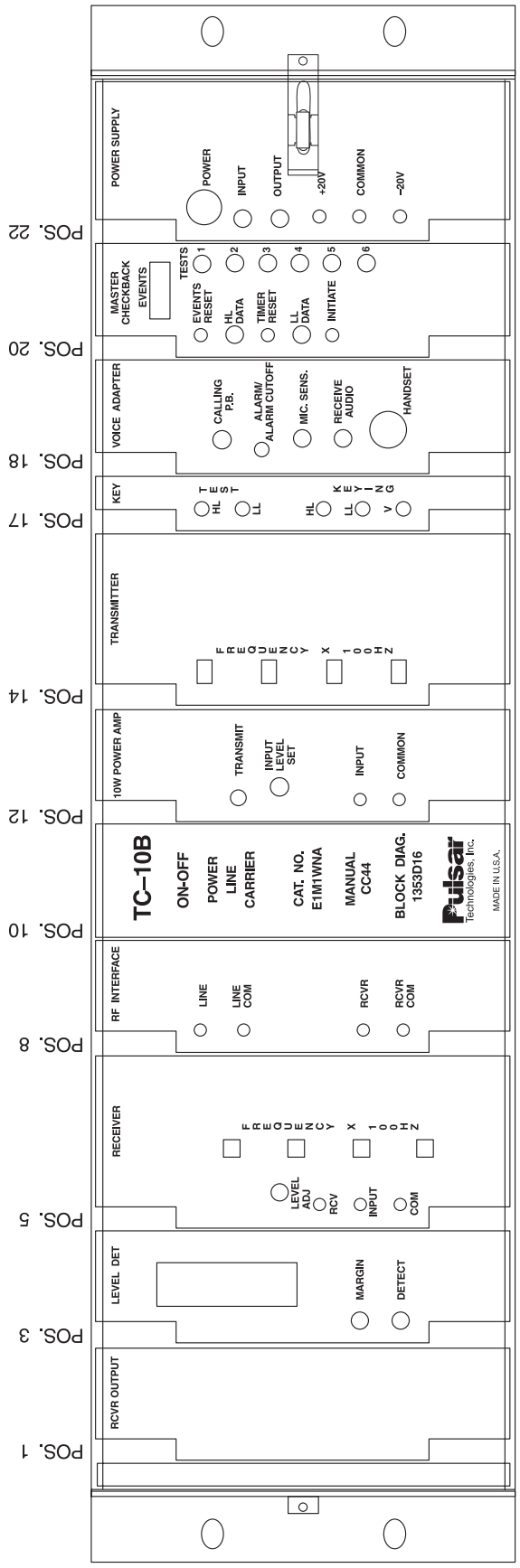


Figure 1–1. TC–10B Chassis and Control Panels with Optional Automatic Checkback (Master) and Voice Adapter Modules. (1354D16A)

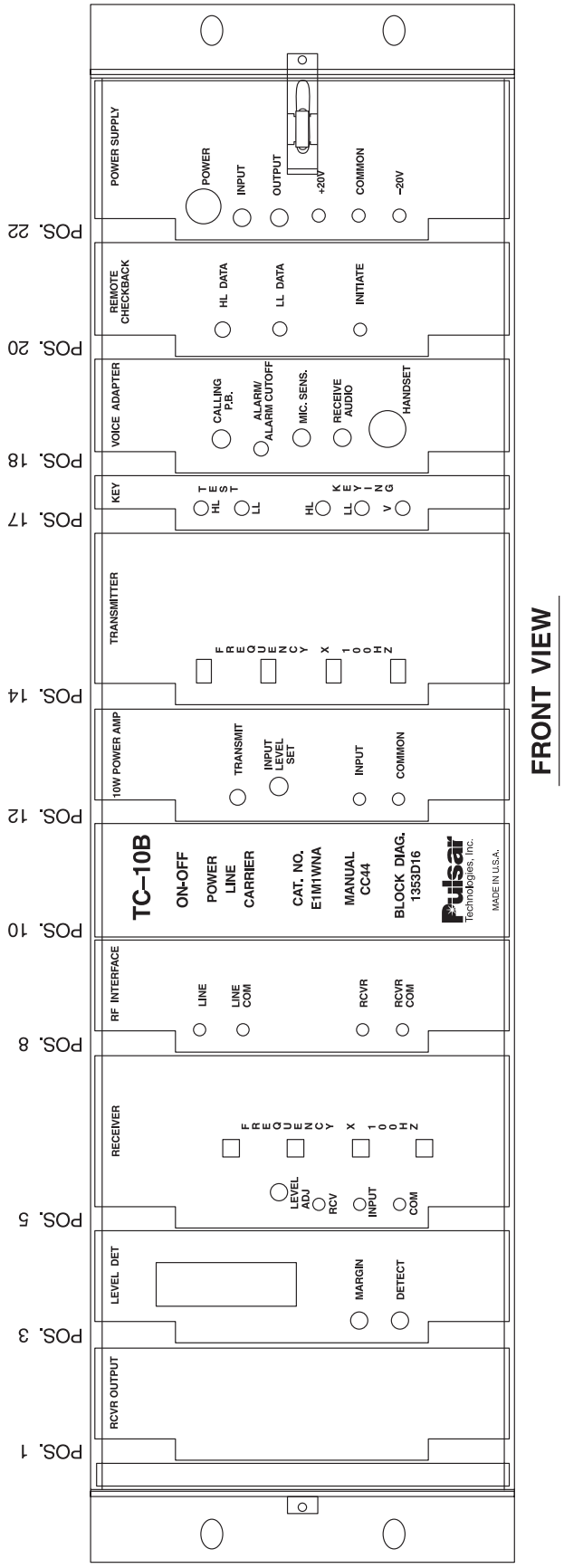


Figure 1–2. TC–10B Chassis and Control Panels, Showing Optional Remote Automatic Checkback Module. (1354D16C)

1.5.3 Receiver Outputs

Table 1-3 shows the TC–10B Receiver Output Specifications.

Table 1–3. Receiver Output Specifications.

Two independent relaying outputs	Both outputs (fully isolated) provide up to 1 A transistor switch for microprocessor relaying or 200 mA (into 24 ohms), 20 mA (into 2,200 ohms); will operate from any battery supply (38 to 280 Vdc)
One receive alarm output	One Form A Mercury-wetted 100 VA, 125 Vdc (maximum)
One carrier level output (optional)	0–100 μA for external indicator

1.5.4 Alarm & Level Option

Table 1-4 shows Alarm & Level Option specifications for the TC–10B.

Table 1–4. Alarm & Level Option Specifications.

Alarm Contacts (dc Power Loss, RF "ON", and Receive at Margin; 3 separate relays)	Form A or B contacts (field strappable) rated 100 VA; 0.5 sec and dropout delay
Carrier Level Indication Meter Reading	–20 dB to +10 dB

1.5.5 Checkback Option

Table 1-5 shows the TC–10B checkback option specifications.

Table 1–5. Checkback Option Specifications.

Master	• Programmable for checkback interval, test sequence, and number of remotes (up to 3) • Alarm contacts for failures • Optional events counter with battery backup
Remote	• Remote initiate feature generates a complete master test sequence • Slave remotes may be "Daisy-Chained" for multiple carrier connections

1.5.6 Voice Adapter Option

Table 1-6 shows the TC–10B Voice Adapter Option specifications.

Table 1–6. Voice Adapter Option Specifications.

Modulation	Amplitude Modulation with compandor
Transmission	Half-Duplex
Frequency Response	300 Hz to 2 kHz
Signaling	Carrier alarm

1.5.7 Environmental

Table 1-7 shows the TC–10B environmental specifications.

Table 1–7. Environmental Specifications.

Ambient temperature range of air-contacting equipment	-20 to +60°C (derated per Table 1-9) (ANS C37.90.)
Relative humidity	Up to 95% (non-condensing) at 40°C (for 96 hours cumulative) (ANS/UL 508)
Altitude	• Up to 1,500 m (without derating) • Up to 6,000 m (using Table 1-8 and Table 1-9)
SWC and FAST Transient	All external user interfaces meet SWC and FAST Transients of ANS C37.90.1 and IEC 255-6
Dielectric	Only isolated inputs and outputs, and all alarms: 2,500 Vdc from each terminal to ground, derated per Table 1-8. (IEC 255-5)
Center conductor of coaxial cable to ground	3,000 Vdc impulse level, using 1.2 x 50 msec impulse
Electro-Magnetic Interference Compatibility:	IEEE Trial-Use-Standard P734/D5/R4 (ANS C37.90.2).

Table 1–8.
Altitude Dielectric Strength
De-Rating for Air Insulation

Altitude (Meters)	Correction Factor
1,500	1.00
1,800	0.97
2,100	0.94
2,400	0.91
2,700	0.87
3,000	0.83
3,600	0.79
4,200	0.74
4,800	0.69
5,400	0.64
6,000	0.59

Table 1–9.
Altitude Correction For Maximum
Temperature Of Cooling Air (ANS C93.5).

		Temperatures (Degrees C)		
Altitude (Meters)		Short-Time	Long-Time	Difference From Usual
Usual	1,500	55	40	—
Unusual	2,000	53	38	2
Unusual	3,000	48	33	7
Unusual	4,000	43	28	12

1.5.8 Power Requirements and Dimensions

Table 1-10 shows the TC–10B power requirement specifications.

Table 1–10. Power Requirement Specifications.

Transceiver		Supply Current (Amps) At Nominal Voltage		
Nominal Battery Voltage	Permissible Voltage Range	Receive/ Standby	1 Watt Transmit	10 Watt Transmit
48/60 Vdc	38–70 Vdc	.630	.940	1.600
110/125 Vdc	88–140 Vdc	.240	.360	.600
220/250 Vdc	176–280 Vdc	.120	.180	.300

Table 1-11 shows the TC–10B weight and dimension specifications.

Table 1–11. Weight and Dimension Specifications.

Equipment	Net Weight		Height		Width		Depth		Rack
	lbs	Kg	inches	mm	inches	mm	inches	mm	Space
Transceiver	21	9.53	5.25	133.4	19.00	482.6	13.50	342.9	3 RU

1.6 Circuit Considerations

Primary control circuits for the TC–10B are the crystal-controlled oscillators located in the Transmitter and Receiver modules. These oscillators perform two functions:

- Determine frequency stability
- Provide reference signals for the Receiver Synthesizer

The Synthesizer permits more than 1,000 channel settings, between 30 kHz and 535 kHz, in 0.5 kHz steps. The Synthesizer (phase-lock-loop design) can be adjusted quickly in the field, and can be tuned accurately without test equipment.

The channel speed of the relaying function is determined by the bandwidth and the amount of signal overdrive:

- With 15 dB margin above the receiver threshold, wideband (1,200 Hz) requires 2.5 ms detect (or pickup) time, and 2.5 ms release (or dropout) time; the end-to-end operating time includes:
  - Transmitter sending signal
  - Receiver receiving and recognizing signal
  - Receiver operating solid state output
  - Solid state output sending signal
- Narrowband (600 Hz) requires 3.6 ms detect (or pickup) time, and 3.6 ms margin (or dropout) time.

The transmitted modulated signal is band-limited, i.e., the frequency spectrum is limited to the channel bandwidth.

If you are using the Voice Adapter module, it will have an independent receiver (4 kHz bandwidth), regardless of whether the system is operating at 1,200 Hz (wideband) or 600 Hz (narrowband).

The standard 10 watt output may be reduced to as little as 0.1 watt. Receiver sensitivity is 60 mV (wideband) and 20 mV (narrowband), allowing operation on longer lines without an external amplifier.

The chassis is prewired for all options which are supplied as plug-in modules, and the mounting flange is adjustable to vary the mounting depth. All inputs and outputs are optically isolated and connect to rear mounted terminal blocks.

Universal buffered keying input is provided for electro-mehanical, solid-state, or microprocessor pilot relay systems. Universal outputs are also provided for electro-mehanical or solid-state systems.

USER NOTES

Chapter 2. Applications and Ordering Information

2.1 Protective Relay Applications Using ON/OFF Carriers

The TC–10B carrier set is particularly suitable for the following types of protective relay systems:

- Directional-Comparison Blocking
- Phase-Comparison Blocking
  - Current Only
  - Distance Supervised

2.1.1 Directional-Comparison Blocking

The basic elements for directional-comparison blocking systems are shown in Figure 2-1a and Figure 2-1b. At each terminal, the phase and ground trip units (P) must be directional and set to overreach the remote terminal; that is, they must be set to operate for all internal faults. Nominal settings of the distance units are 120 to 150 percent of the line. The start units (S) must reach farther, or be set more sensitively, than the remote trip units. Thus S_1 must be set more sensitively than P_2 or reach farther behind bus G. Likewise, S_2 must be set more sensitively than P_1 or reach farther behind bus H. In any case, the S and P relays should be similar in type. If the trip unit (P) is a directional overcurrent ground relay, the start (S) ground relay should be a similar non-directional overcurrent unit. The same principle applies for the phase relays.

When the TC–10B ON-OFF power line carrier is used with these schemes, except for possible auxiliary functions, **no signal is normally transmitted**, since the S units operate only during fault conditions.

Operation of the directional-comparison scheme (shown in Figure 2-1a and Figure 2-1b) is internal faults. Subscript 1 indicates relays at station G for breaker 1; subscript 2, relays at station H for breaker 2. (Figure 2-1c shows a solid-state logic version of Figure 2-1b.)

The scheme shown in Figure 2-1 is still widely used for its flexibility and reliability. Since the communication channel is not required for tripping, internal faults that might short and interrupt the channel are not a problem. Overtripping will occur, however, if the channel fails or is not established for external faults within the reach of the trip fault detectors. Since the carrier transmitter is normally OFF, or non-transmitting, channel failure cannot be detected until the system is tested or until an external fault occurs. This limitation can be overcome by using the optional TC–10B checkback system with the TC–10B carrier.

2.1.2 Phase-Comparison Blocking

Basic elements of the phase-comparison systems are shown in Figure 2-2. The system uses a composite sequence current network to provide a single-phase voltage output proportional to the positive, negative, and zero sequence current input. Sensitivity to different types of faults depends on the weighting factors or constants designed into the sequence current network. Adjustments to the network are provided.

A squaring amplifier in the controlling relay converts the single-phase voltage output to a square wave. The positive voltage portion corresponds to the positive half-cycle of the filter voltage wave and the zero portion corresponds to the negative half-cycle. The square wave is used to key the TC–10B, transmitting to the remote terminal. The square wave from the remote terminal is compared to the local square wave, which has been delayed by an amount equal to the absolute channel delay time. This comparison of

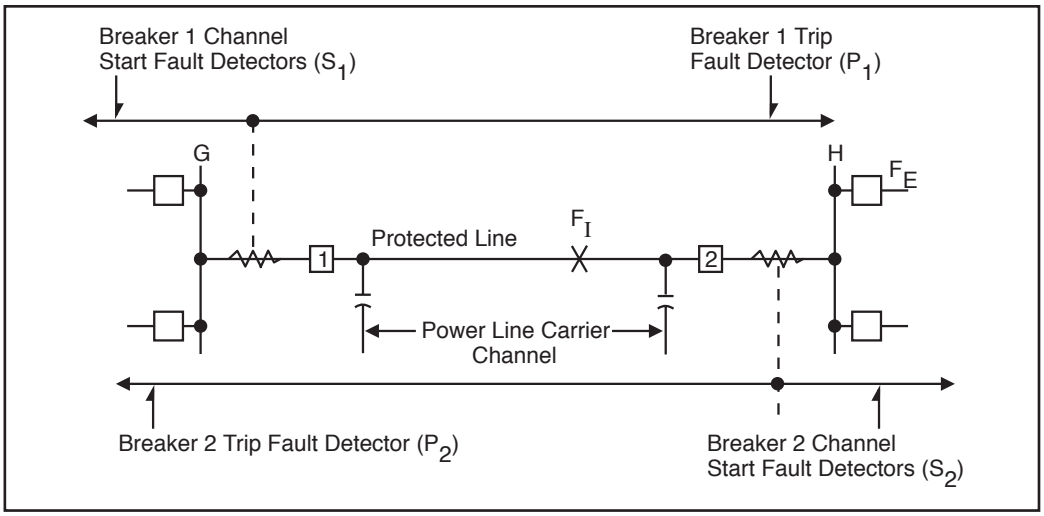


Figure 2–1a. Basic Elements.

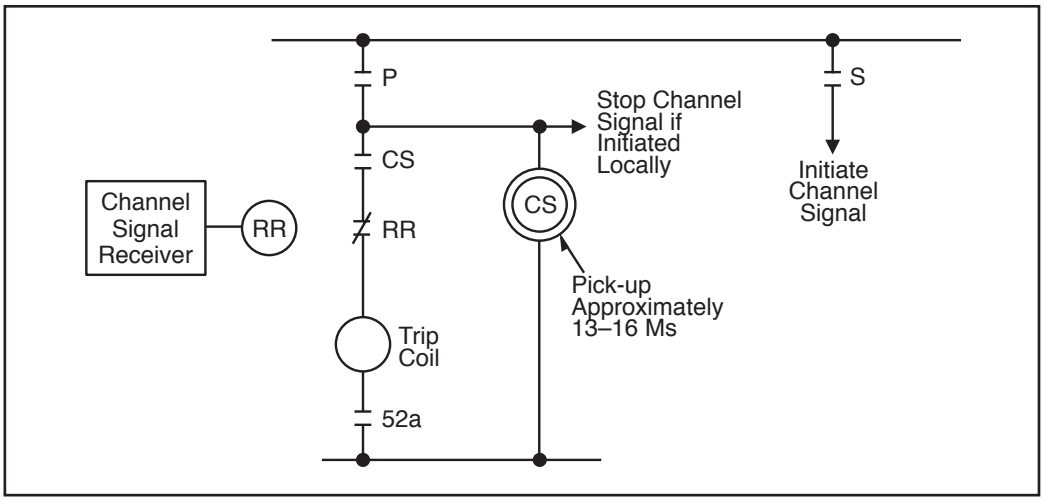


Figure 2–1b. Contact Logic (per Terminal).

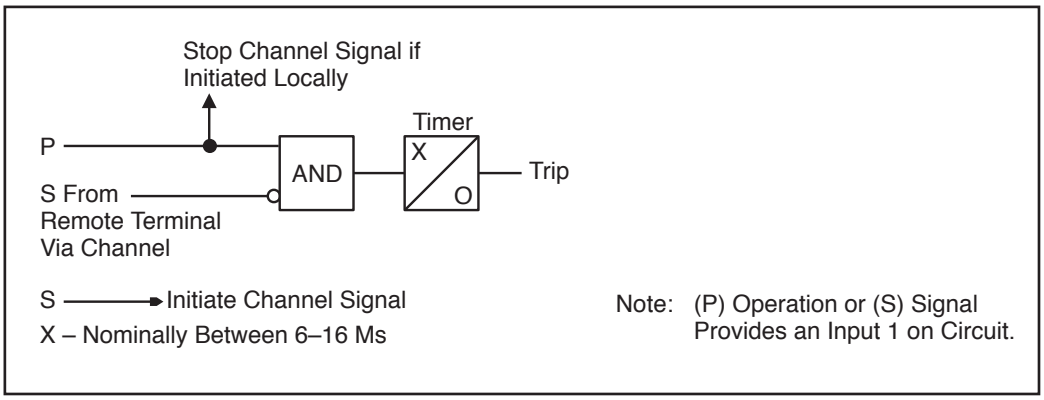


Figure 2–1c. Solid State Logic (per Terminal).

Figure 2–1. Directional-Comparison Blocking, Basic Elements and Logic Diagrams.

Table 2–1. Directional Comparison Schemes for External and Internal Faults.

SCHEME FOR EXTERNAL AND INTERNAL FAULTS		
Type of Fault	**Events at Station G**	**Events at Station H**
External (F_E) For external faults, the CS unit or timer x/o assure that a blocking signal is established.	P_1 operates; S_1 does not see fault. Blocking signal received from station H. RR back contacts open (or 1 signal negates AND). No trip.	S_2 operates to key transmitter. Blocking signal sent to station G. P_2 does not see fault. No trip.
Internal (F_I)	P_1 operates; S_1 may or may not operate, but P_1 operation prevents transmission of a blocking signal. Breaker 1 tripped.	P_2 operates, S_2 may or may not operate but P_2 operation prevents transmission of a blocking signal. Breaker 2 tripped.

* For external faults, the CS unit or timer x/o assure that a blocking signal is established.

the local and remote square waves at each terminal determines whether a fault is internal or external.

Fault detectors are used to determine whether a fault has occurred and to supervise tripping. The fault detectors must be overreaching, i.e., set sensitively enough to operate for all internal phase and ground faults.

Because overcurrent fault detectors are normally used, voltage transformers are not required. Such a scheme is current only. Fault detectors should be set above maximum load, yet operate for all internal faults. Distance fault detectors, which require voltage transformers, are used on heavy-loaded or long lines when distance supervision is required.

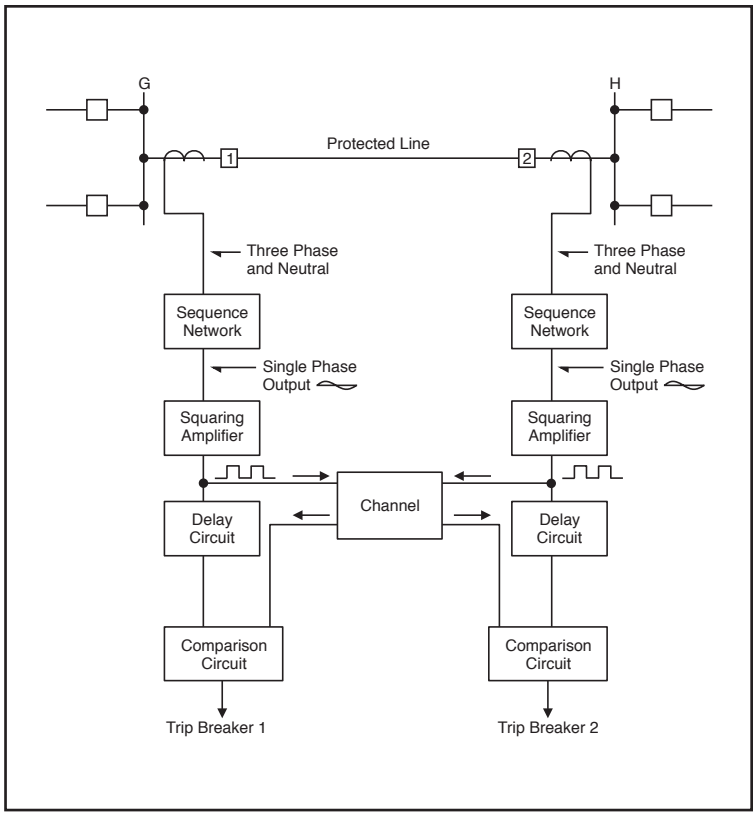


Figure 2–2. Phase-Comparison Blocking, Basic Elements.

2.1.3 Single Phase-Comparison Blocking, Current Only

In the current only system, the TC–10B is used with two overcurrent fault detectors (FD_1 and FD_2). FD_1, the carrier start unit, is set more sensitively than FD_2 and permits the local square wave signal to key the "ON/OFF" carrier transmitter. FD_2, set with a higher pickup than FD_1, is used to arm the system for tripping. For transmission lines less than 100 miles long, the FD_2 pickup is set at 125 percent of FD_1. For lines longer than 100 miles, the FD_2 pickup is set at 200 percent of FD_1. On a three-terminal line, FD_2 is set at 250% of FD_1, provided the line length between any two breakers is less than 100 miles. Phase-Comparison cannot occur until FD_2 operates. The purpose of the two fault detectors is to coordinate the comparison of the local and remote square waves with the keying of the carrier square wave. **The carrier must be started before the comparison is allowed** to ensure that the remote square wave has been received.

The basic operation of the system is shown in Figure 2-3. FD_1 and FD_2 at both terminals operate for an internal fault (F_I). The square wave inputs to the AND from the local currents are essentially in phase with those transmitted via the channel from the remote terminal. The local square wave turns the carrier "ON" and "OFF" to provide the square wave receiver output for the remote terminal.

A flip flop is energized if the inputs to the AND continue for 4 ms, providing a continuous trip output

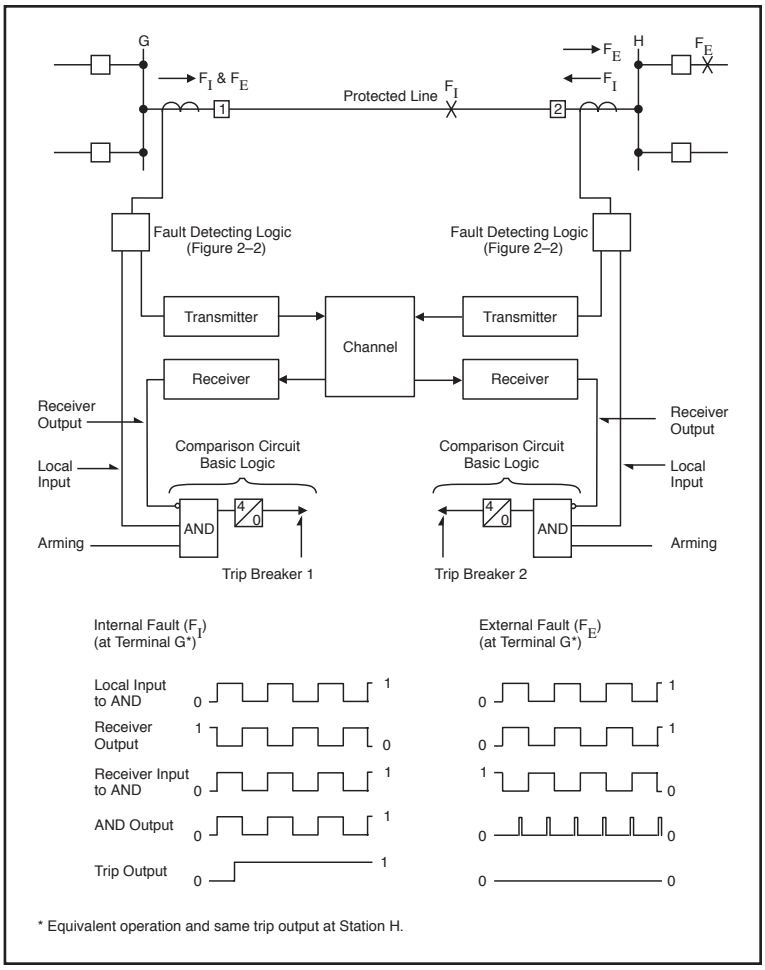


Figure 2–3.
Single Phase Comparison Blocking, Current Only Operation.

supervised by FD_2 operation. The 4 ms correspond to a phase angle difference of 90°, on a 60-Hz base, between the currents at the two terminals. The currents at the two ends of the line may be out of phase by up to 90° and still trip. This is a blocking system, since the receipt of a signal from the channel prevents tripping. The carrier signal, therefore, does not have to be transmitted through the internal fault. No received signal puts a "1" on the AND input. With the remote terminals open, this system provides sensitive instantaneous overcurrent protection for the entire line. As is characteristic of blocking systems, the channel is not required for tripping on internal faults.

For an external fault, such as F_E in Figure 2-3, blocking is essentially continuous, since the remote wave input to the AND is out-of-phase with the local square wave. The secondary ct currents are essentially out-of-phase for an external fault. The currents can, however, be in-phase by up to 90° on a 60-Hz base and still block.

2.1.4 Single-Phase, Distance-Supervised Comparison Blocking

A distance-supervised scheme should be used if the minimum internal three-phase fault current is less than twice the maximum load current. Twice maximum load current allows FD1 to operate positively on the minimum internal three-phase fault, yet reset when an external fault is followed by a maximum load current flowing through the line. The TC–10B operates in the same manner as when used with the current-only scheme, except for the fault detection and arming techniques.

Two sequence current networks and two distance relays supplement the two overcurrent fault detectors.

One sequence current network responds only to negative and zero sequence currents, detecting all phase-to-phase and ground faults (but not three-phase faults). The output of this adjustable network operates the conventional overcurrent FD1 and FD2 fault detectors. The two distance relays operate only for three-phase faults. Thus, FD2 provides the arming function for all unbalanced phase and ground faults, through the adjustable filter, and one of the distance relays (21P) provides arming for all three-phase faults.

The second and non-adjustable sequence current network operates through the squaring amplifier, providing the local square wave and the carrier-keyed square wave required for phase comparison. This signal is keyed by FD1 and the second distance relay (21S) to provide the carrier start functions. This second network responds to positive, negative, and zero sequence currents. Separate networks provide greater sensitivity: with phase-to-phase faults, for example, more than twice the sensitivity is gained.

The setting coordination of FD1 and FD2 overcurrent units is the same as for the current-only system. Settings for the two three-phase distance units are shown in Figure 2-4. Both 21S and 21P distance relays must be set to overreach both the local and remote terminal buses; 21S must be set further than 21P, as shown.

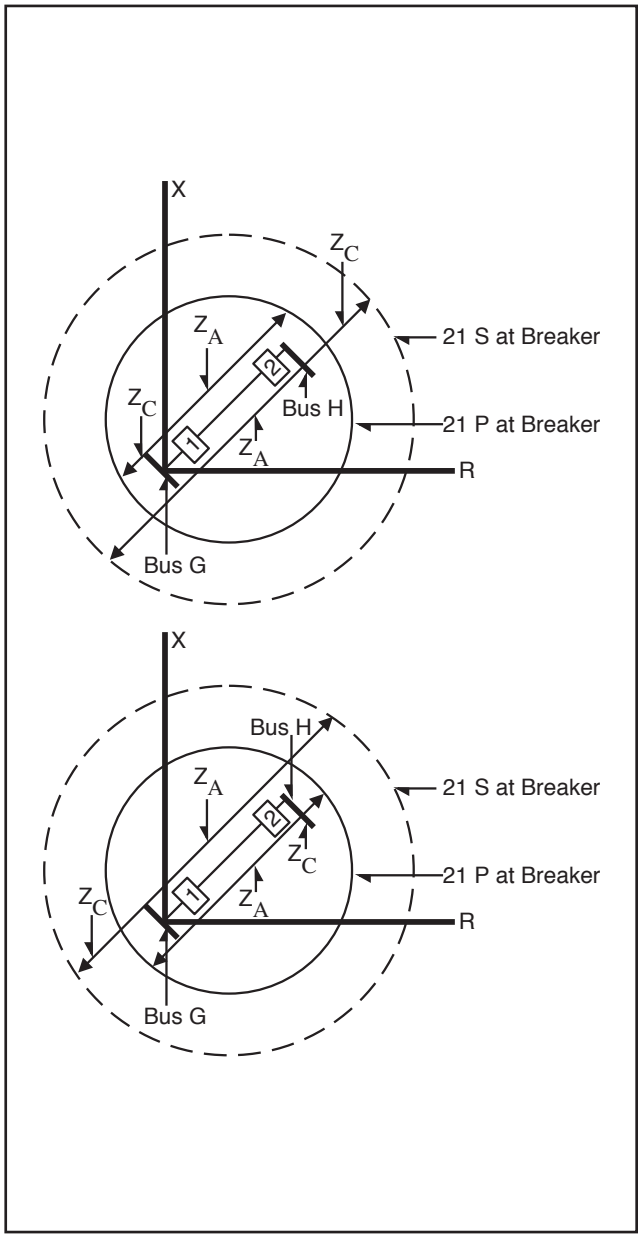


Figure 2–4. Single Phase-Comparison Blocking, Distance-Supervised Operation.

2.2 Special Application Considerations

Because the TC–10B is "ON/OFF" modulated, only one frequency (f_C) is required for line protection. When applied to three terminal lines, phase cancellation will occur when two or more transmitters are keyed simultaneously. To prevent this, you should offset transmitters by ±100 Hz, using the thumbwheel frequency programming switches. The three frequencies should be:

- f_C
- f_C - 100 Hz
- f_C + 100 Hz

When using the TC–10B with the SKBU-1 Phase-Comparison, you must offset the transmitter frequencies from the center frequency by 100 Hz for all applications. In a two-terminal application, set the transmitter at one end 100 Hz above the center frequency, and the transmitter at the other end 100 Hz below the center frequency. Thus, the two transmitters are spaced 200 Hz from each other. For a three terminal line, you should offset the transmitter as described in the above paragraph.

The TC–10B does not have an adjustable filter or hybrid attached to the output of the transmitter. If you are using the TC–10B in an application where no other power line carrier equipment is attached to the power line, then no further action is required. **However, in the application of Single Comparator Phase Comparison relaying, the TC–10B is to be operated in the four-wire mode (see RF Interface Module), with an external skewed hybrid between transmitter and receiver.**

If you are applying the carrier set with other transmitters, coupled through the same tuning equipment, you must apply a hybrid or a series LC unit to the transmitter output to isolate the other transmitters from the TC–10B transmitter. This will avoid the problems of intermodulation distortion. We suggest that you use a hybrid if the frequency spacing between all transmitters is within the bandwidth of the hybrid (usually 6%). Check the manufacturers instructions for the actual spacing limitations of the hybrid you are using. If you cannot use a hybrid, then you may use a series LC unit to isolate the transmitters. In this case, the transmitters must have spacing such that the LC you are using will attenuate the external frequencies by at least 20 dB (if the other frequency is a 10 watt transmitter), and 30 dB (if the other frequency is a 100 watt transmitter).

2.3 Ordering Information

The TC–10B carrier is functionally compatible with earlier type carrier equipment (e.g., KR, TC, TC-10, TC-10A). That is, you may use the TC–10B with these other carrier types at the opposite end of the line, with or without voice function. You may use the same telephone handset unit with any of these ON-OFF carrier sets.

You may use the TC–10B carrier set with the following types of relay systems:

- All Directional-Comparison Blocking Systems
- Phase-Comparison Blocking Systems, e.g., SKBU-1 **(Requires 45-Vdc power supply — please see Table 2-5.)**

Simplified schematics of typical electro-mechanical systems are shown in Figure 2-5 through Figure 2-13 (schemes A thru K). These schemes indicate the different jumper positions required for particular applications. Simplified connections between the TC–10B and a microprocessor based relay are shown in Figure 2-14 (Scheme L).

Figure 2-15 shows the resultant output circuit when the external resistors are required for 125 and 250 Vdc systems.

Three TC–10B options are available:

(1) Plug-in Voice Adapter Module with signaling as a push-to-talk maintenance voice channel - (see Chapter 18). A telephone jack is provided on the Voice Adapter Module, but you may also use a remote jack or hookswitch. (See Figure 18-4, Scheme J, for the connection diagrams.)

(2) Plug-in (Master/Remote) Automatic Carrier Checkback Module for periodic testing of the carrier channel at programmable intervals (see Chapter 17). (See Figure 3–3 for connection diagrams.)

(3) Alarm and Carrier level indication, includes:

- Loss of Vdc alarm
- Transmit power monitor alarm
- Received power margin alarm
- Instrument indicating carrier level (–20 dB to +10 dB)
- Output for external carrier level indicator (0–100 μA)

The equipment identification number (catalog number) is located in the middle of the front panel (just to the left of the 10W PA Module). The TC–10B catalog number comprises eight (8) characters, each in a specific position. This number identifies the uniut's technical characteristics and capabilities, as well as any optional modules installed in the unit.

Table 2-2 provides a complete listing of the options for ordering a TC–10B, as well as a sample catalog number. To order one or more TC–10Bs, simply identify the features and optional modules you want for each chassis. For example, the typical catalog number shown in Table 2-2 — E 1 M 1 W V A S — orders a TC–10B with the following features:

Basic TC–10B Transmitter/Receiver

Power Output: 10 watt

Automatic Checkback: Master Checkback Module with Event Counter

dc/dc Converter Power Supply: 110/125 Vdc battery input

Bandwidth (Filter Range): Wideband filter

Voice Adapter: Voice Adapter Module with signaling

Alarm and Carrier Level Indication: with loss-of-dc-power alarm relay, R.F. output alarm relay, received-carrier-level-margin alarm relay, carrier level analog output (0–100 μA) for external instrument

Outputs: Dual transistor-switched outputs (for use with electromechanical carrier auxiliary relays and microprocessor relays)

Table 2-3 provides a further breakdown of the TC–10B catalog number by style numbers.

The accessories avaialable for the TC–10B are listed, along with their style numbers, in Table 2-4 and Table 2-5. To order an accessory, simply give its style number.

Table 2–2. TC–10B Catalog Numbers

Catalog Number Position	1	2	3	4	5	6	7	8
Typical Catalog Number	**E**	**1**	**M**	**1**	**W**	**V**	**A**	**S**

Basic TC–10B Transmitter/Receiver

Solid state programmable transmitter/receiver assembly for phase- or directional-comparison relaying, or supervisory control	**E**

Power Output

10 watt output *	**1**

Automatic Checkback

Master Checkback Module with Event Counter	**M**
Master Checkback Module without Event Counter	**C**
Remote Checkback Module	**R**
No Checkback Module	**N**

DC/DC Converter Power Supply

48/60 Vdc battery input	**4**
110/125 Vdc battery input	**1**
220/250 Vdc battery input	**2**

Bandwidth (Filter Range)

Wideband filter	**W**
Narrowband filter	**X**

Voice Adapter

Voice Adapter Module with signaling	**V**
No Voice Adapter Module	**N**

Alarm and Carrier Level Indication

With loss-of-dc-power alarm relay, R.F.-output alarm relay, received-carrier-level-margin alarm relay, carrier level analog output (0–100 μA) for external instrument	**A**
No alarm relays	**N**

Outputs

Dual transistor-switched outputs (for use with electromechanical carrier auxiliary relays and microprocessor relays)	**S**
Dual constant current outputs (20 mA/200 mA/+15 V output with current jacks)	**C**

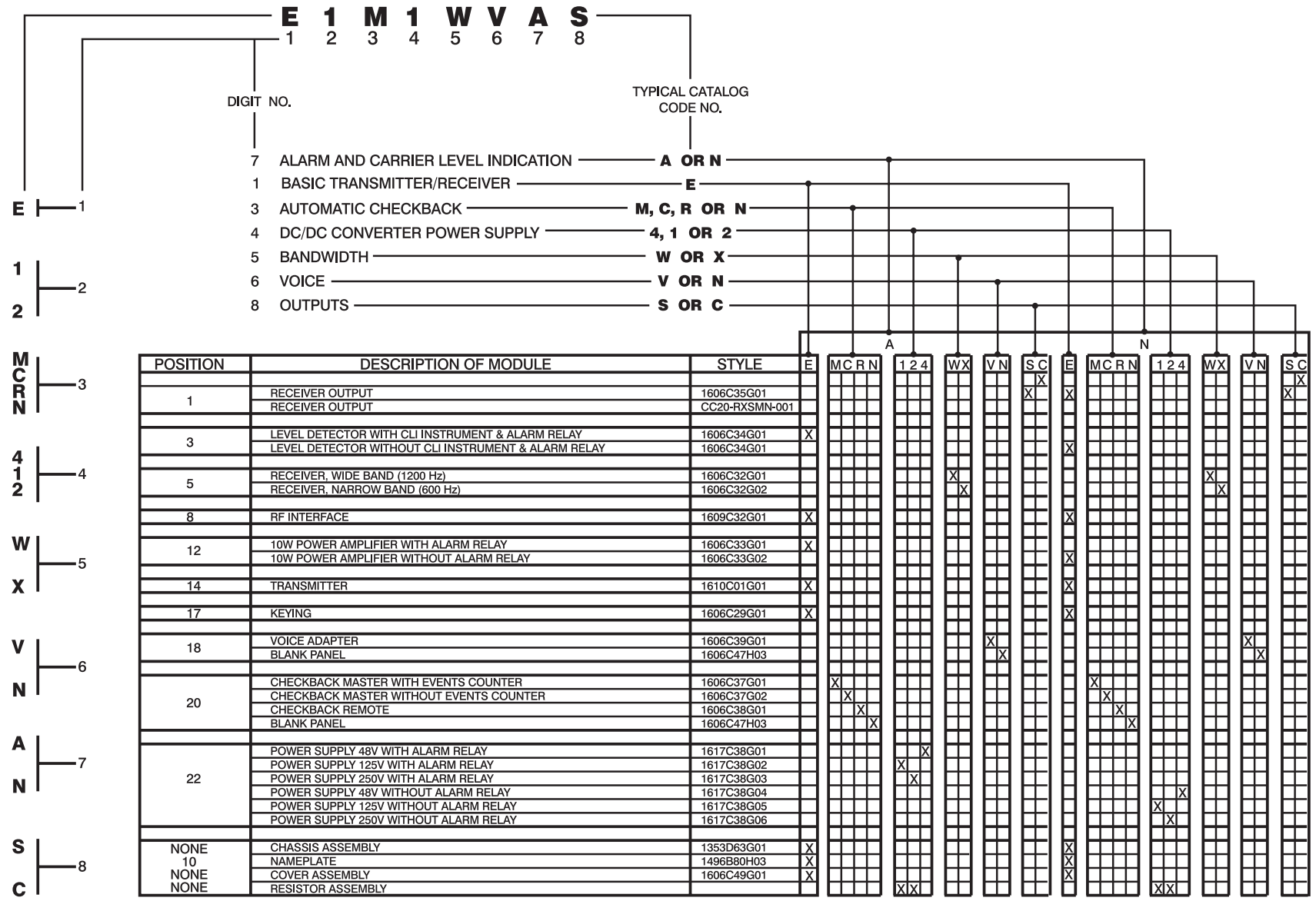
**For 50 or 100 watt output, see separate information on the LPA, Linear Power Amplifier*

Accessories

TC–10B/TCF–10B Extender Board . . . . . .Style # 1353D70G01

TC–10B to KR mounting kit . . . . . .Style # 1355D61G01

Table 2–3. TC–10B Catalog Numbers/Module Style Numbers (1354D16).



POSITION	DESCRIPTION OF MODULE	STYLE	E	M C R N	1 2 4	W X	V N	S C	E	M C R N	1 2 4	W X	V N	S C
1	RECEIVER OUTPUT	1606C35G01						X	X					X
	RECEIVER OUTPUT	CC20-RXSMN-001												
3	LEVEL DETECTOR WITH CLI INSTRUMENT & ALARM RELAY	1606C34G01	X											
	LEVEL DETECTOR WITHOUT CLI INSTRUMENT & ALARM RELAY	1606C34G01							X					
5	RECEIVER, WIDE BAND (1200 Hz)	1606C32G01				X						X		
	RECEIVER, NARROW BAND (600 Hz)	1606C32G02				X						X		
8	RF INTERFACE	1609C32G01	X						X					
12	10W POWER AMPLIFIER WITH ALARM RELAY	1606C33G01	X											
	10W POWER AMPLIFIER WITHOUT ALARM RELAY	1606C33G02							X					
14	TRANSMITTER	1610C01G01	X						X					
17	KEYING	1606C29G01	X						X					
18	VOICE ADAPTER	1606C39G01					X						X	
	BLANK PANEL	1606C47H03					X						X	
20	CHECKBACK MASTER WITH EVENTS COUNTER	1606C37G01		X						X				
	CHECKBACK MASTER WITHOUT EVENTS COUNTER	1606C37G02		X						X				
	CHECKBACK REMOTE	1606C38G01		X						X				
	BLANK PANEL	1606C47H03		X						X				
22	POWER SUPPLY 48V WITH ALARM RELAY	1617C38G01			X									
	POWER SUPPLY 125V WITH ALARM RELAY	1617C38G02			X									
	POWER SUPPLY 250V WITH ALARM RELAY	1617C38G03			X									
	POWER SUPPLY 48V WITHOUT ALARM RELAY	1617C38G04									X			
	POWER SUPPLY 125V WITHOUT ALARM RELAY	1617C38G05									X			
	POWER SUPPLY 250V WITHOUT ALARM RELAY	1617C38G06									X			
NONE	CHASSIS ASSEMBLY	1353D63G01	X						X					
10	NAMEPLATE	1496B80H03	X						X					
NONE	COVER ASSEMBLY	1606C49G01	X						X					
NONE	RESISTOR ASSEMBLY				X						X			

Table 2–4. TC–10B Voice Adapter Accessories.

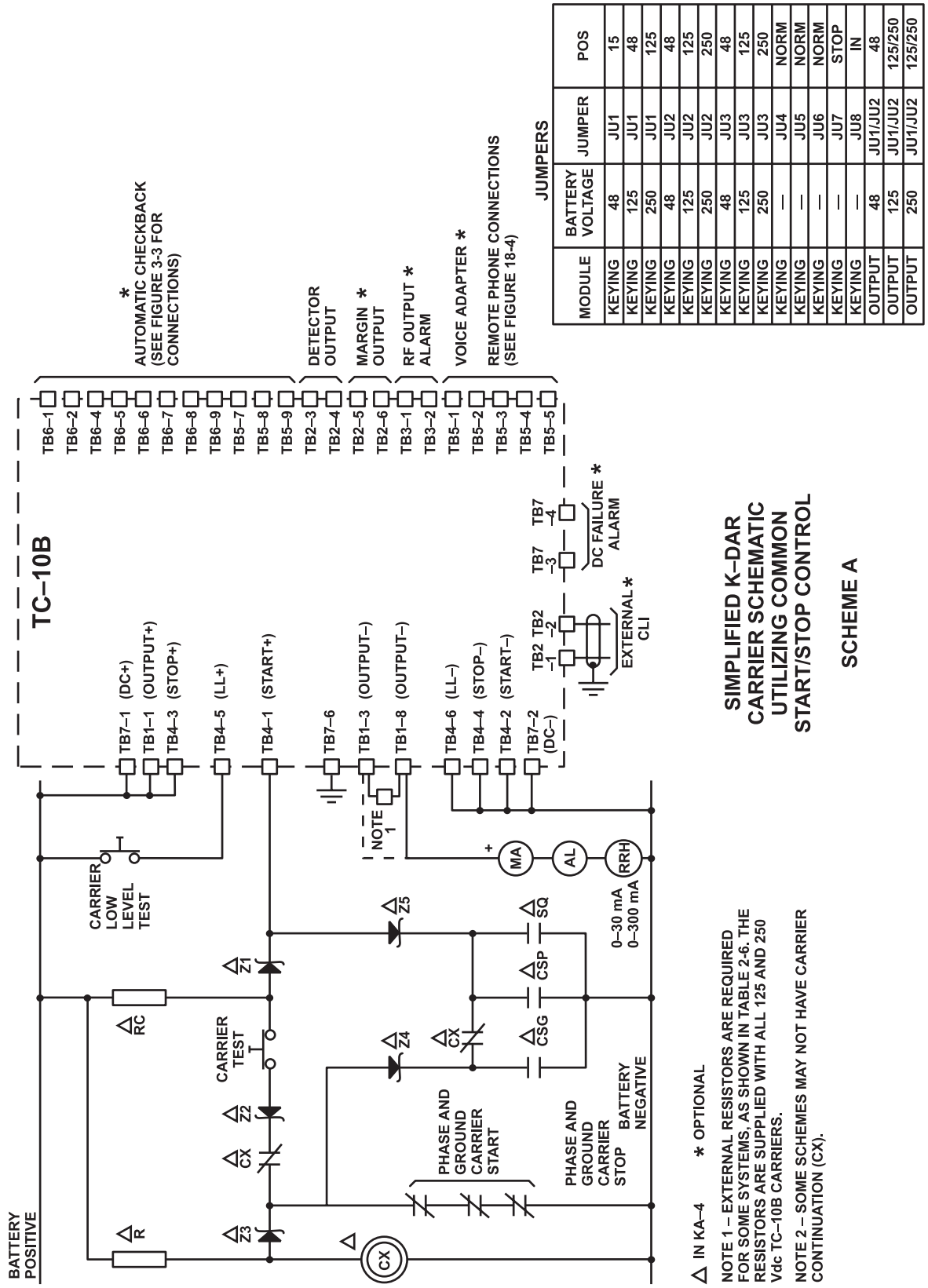
Accessories for Voice Adapter	Style Number
Sonalert (2,900 Hz, 60–250 Vdc)	SC250J
Telephone Hookswitch Assembly (panel mounting) with Noise Canceling Handset	205C266G05
Telephone Handset, Push to Talk, Noise Canceling (single prong plug)	1353D88G01
Telephone Jack, remote panel mounting (single prong plug)	715B674G03

Table 2–5. Other TC–10B Accessories

Other Accessories	Style Number
45 V power supply for use with SKBU-1 Relaying System	
48 V to 45 V	5303D49G05
125 V to 45 V	5303D49G06
250 V to 45 V	5303D49G07

Table 2–6. External Resistor Requirements — Provided with Chassis, According to Battery Voltage.

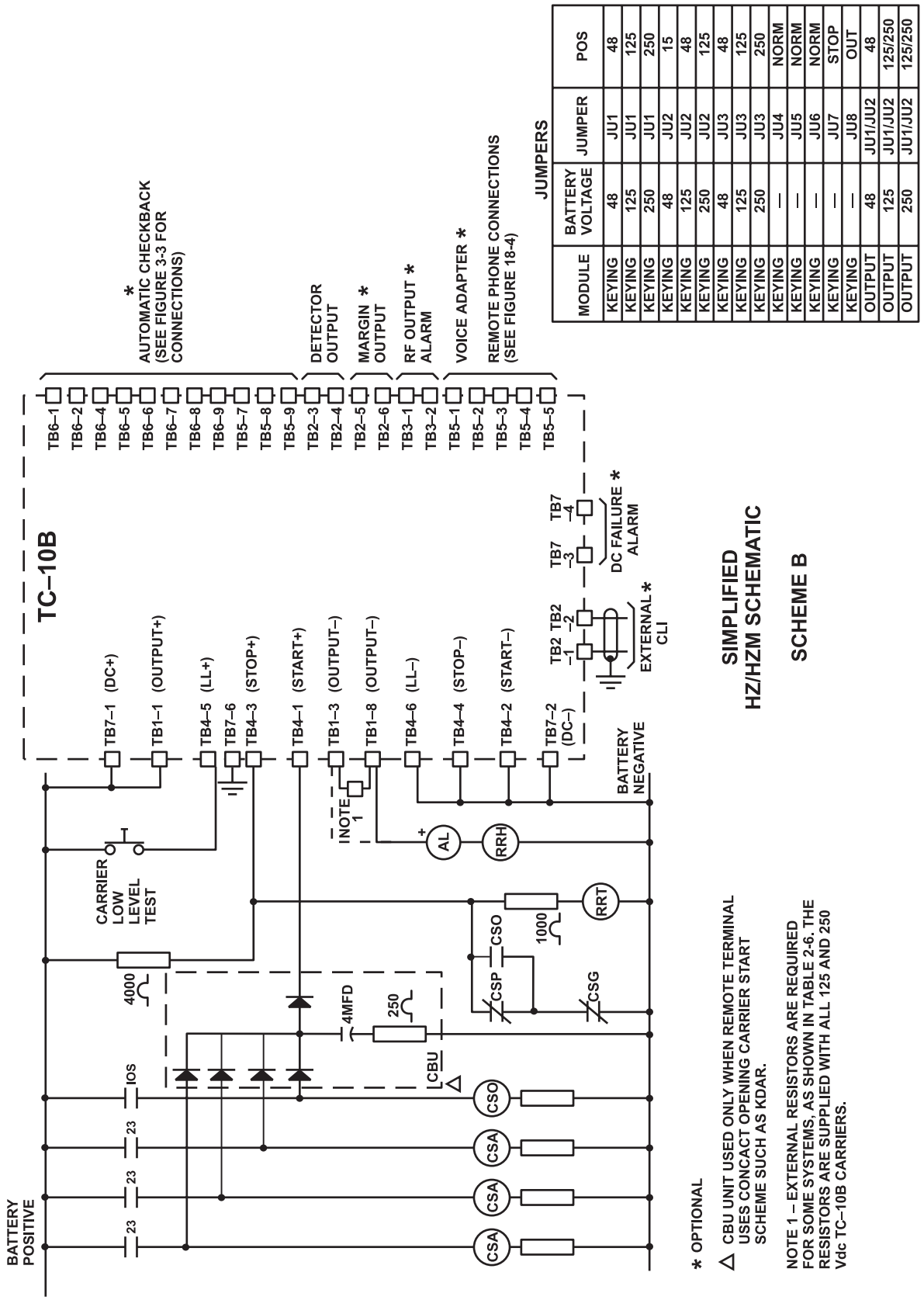
Carrier Aux. Relay	Battery Voltage	Resistor



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	15
KEYING	125	JU1	48
KEYING	250	JU1	125
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	NORM
KEYING	—	JU5	NORM
KEYING	—	JU6	NORM
KEYING	—	JU7	STOP
KEYING	—	JU8	IN
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

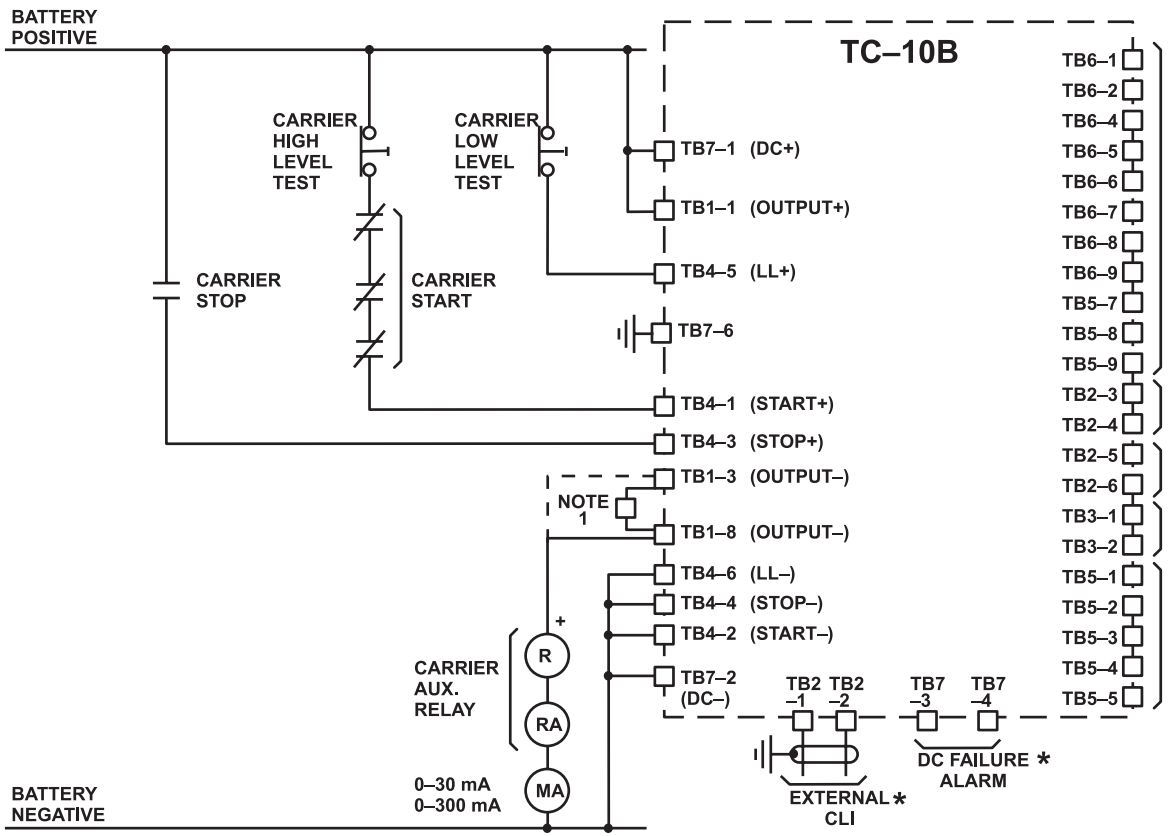
Figure 2–5. TC–10B Simplified Application Schematic – Scheme A (7833C63).



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	15
KEYING	125	JU2	48
KEYING	250	JU2	125
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	NORM
KEYING	—	JU5	NORM
KEYING	—	JU6	NORM
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

Figure 2–6. TC–10B Simplified Application Schematic – Scheme B (7833C63).



* OPTIONAL

NOTE 1 – EXTERNAL RESISTORS ARE REQUIRED FOR SOME SYSTEMS, AS SHOWN IN TABLE 2-6. THE RESISTORS ARE SUPPLIED WITH ALL 125 AND 250 Vdc TC–10B CARRIERS.

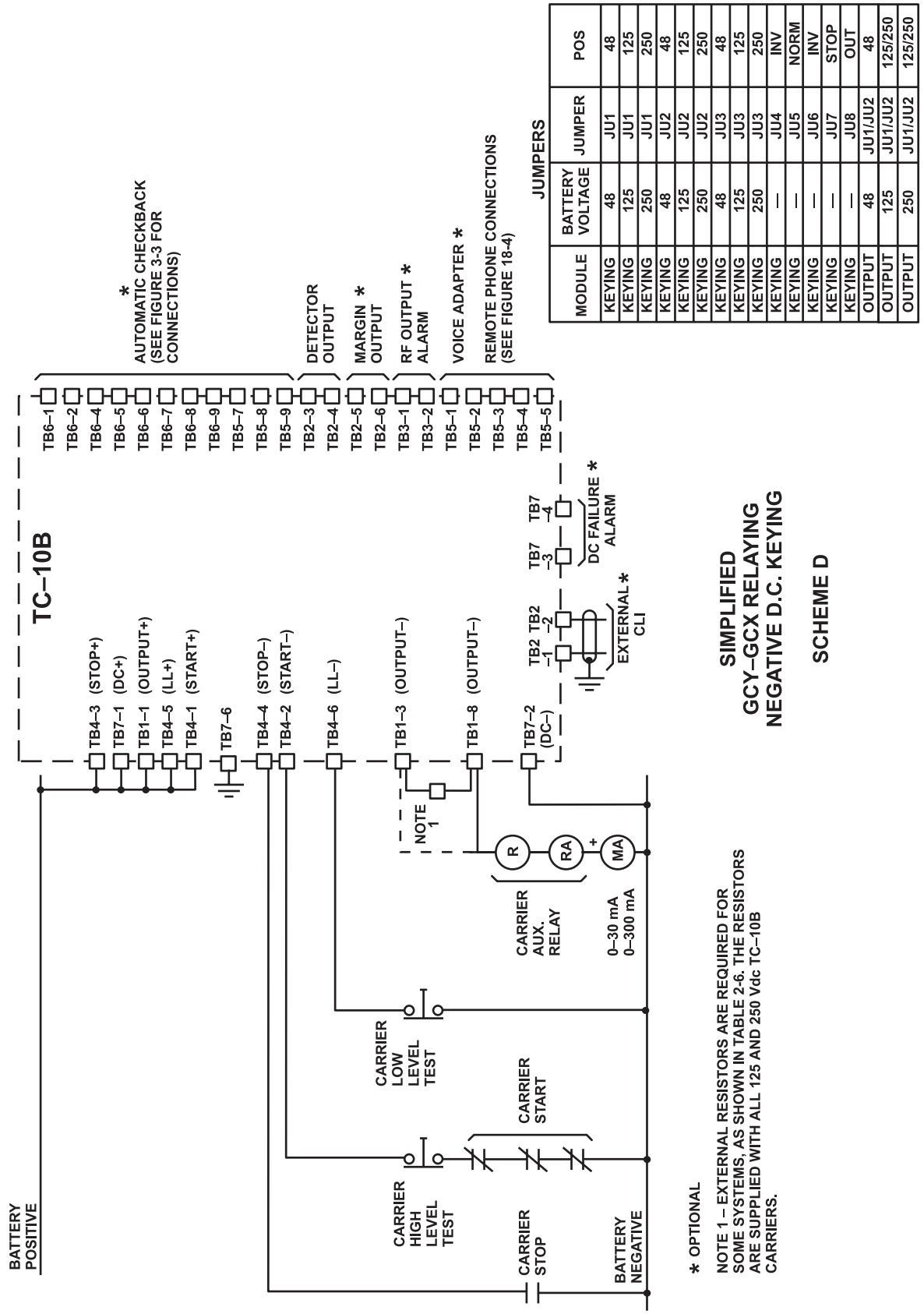
SIMPLIFIED GCY–GCX RELAYING POSITIVE D.C. KEYING

SCHEME C

JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	INV
KEYING	—	JU5	NORM
KEYING	—	JU6	INV
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

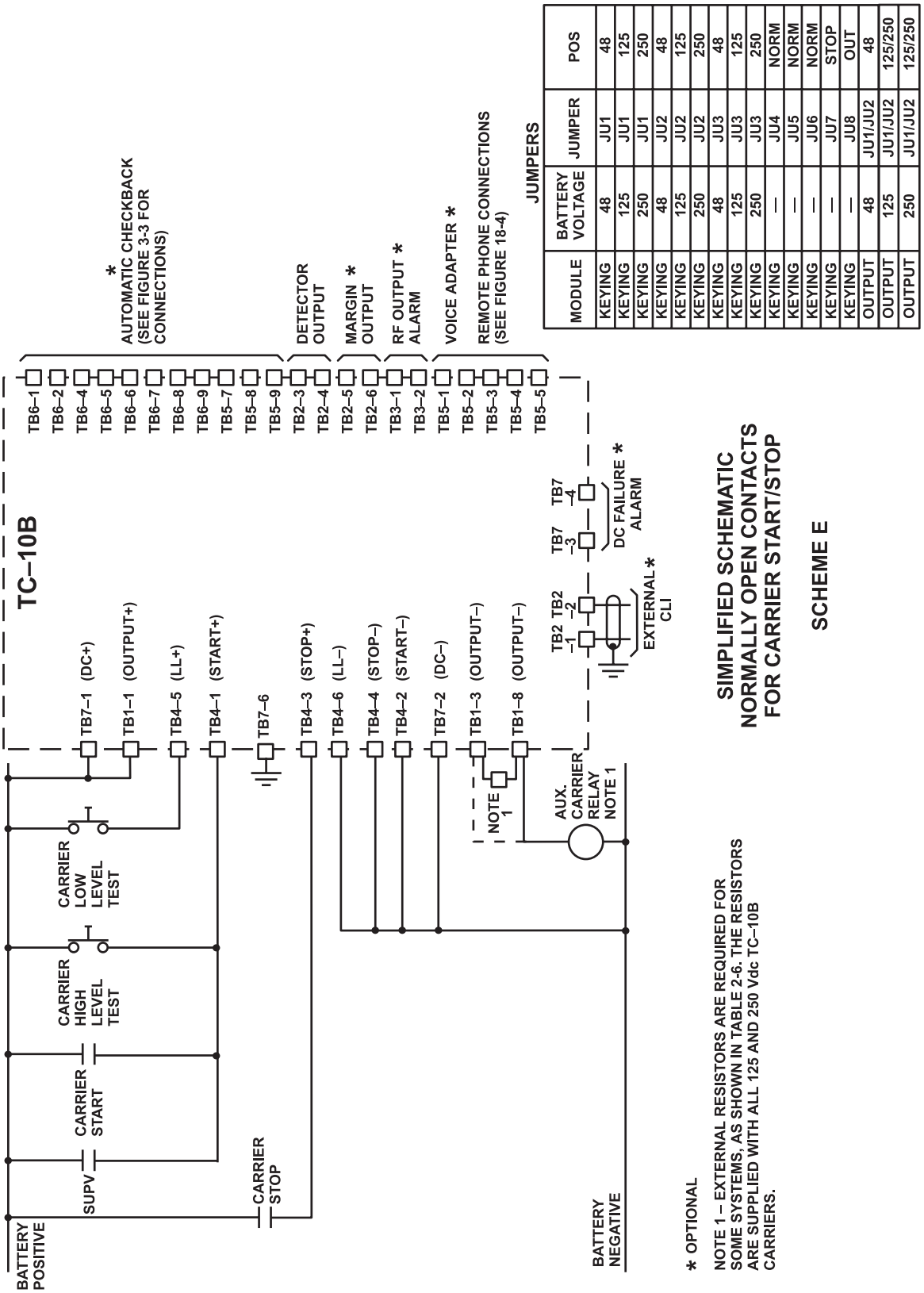
Figure 2–7. TC–10B Simplified Application Schematic – Scheme C (7833C63).



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	INV
KEYING	—	JU5	NORM
KEYING	—	JU6	INV
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

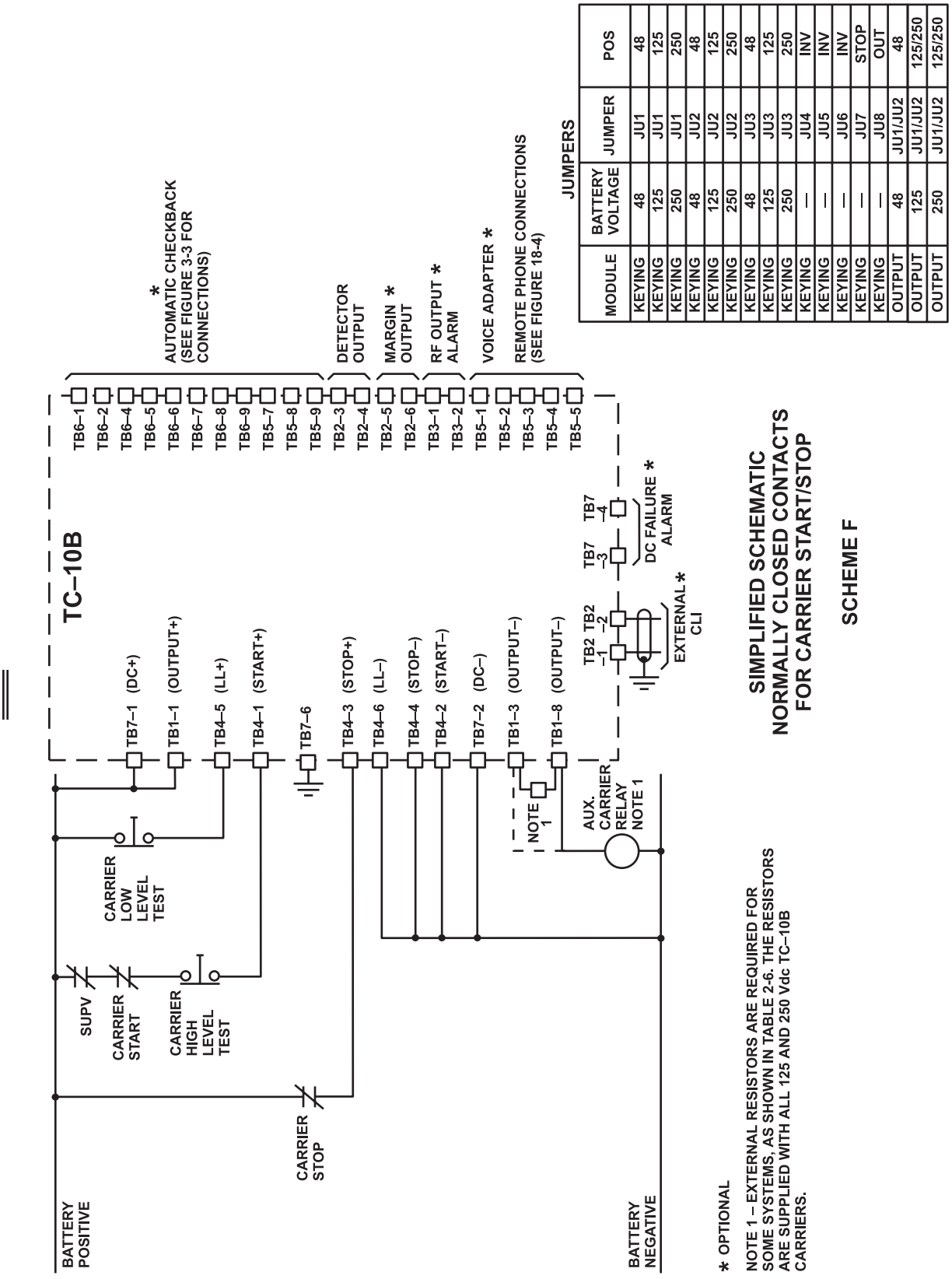
Figure 2–8. TC–10B Simplified Application Schematic – Scheme D (7833C63).



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	NORM
KEYING	—	JU5	NORM
KEYING	—	JU6	NORM
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

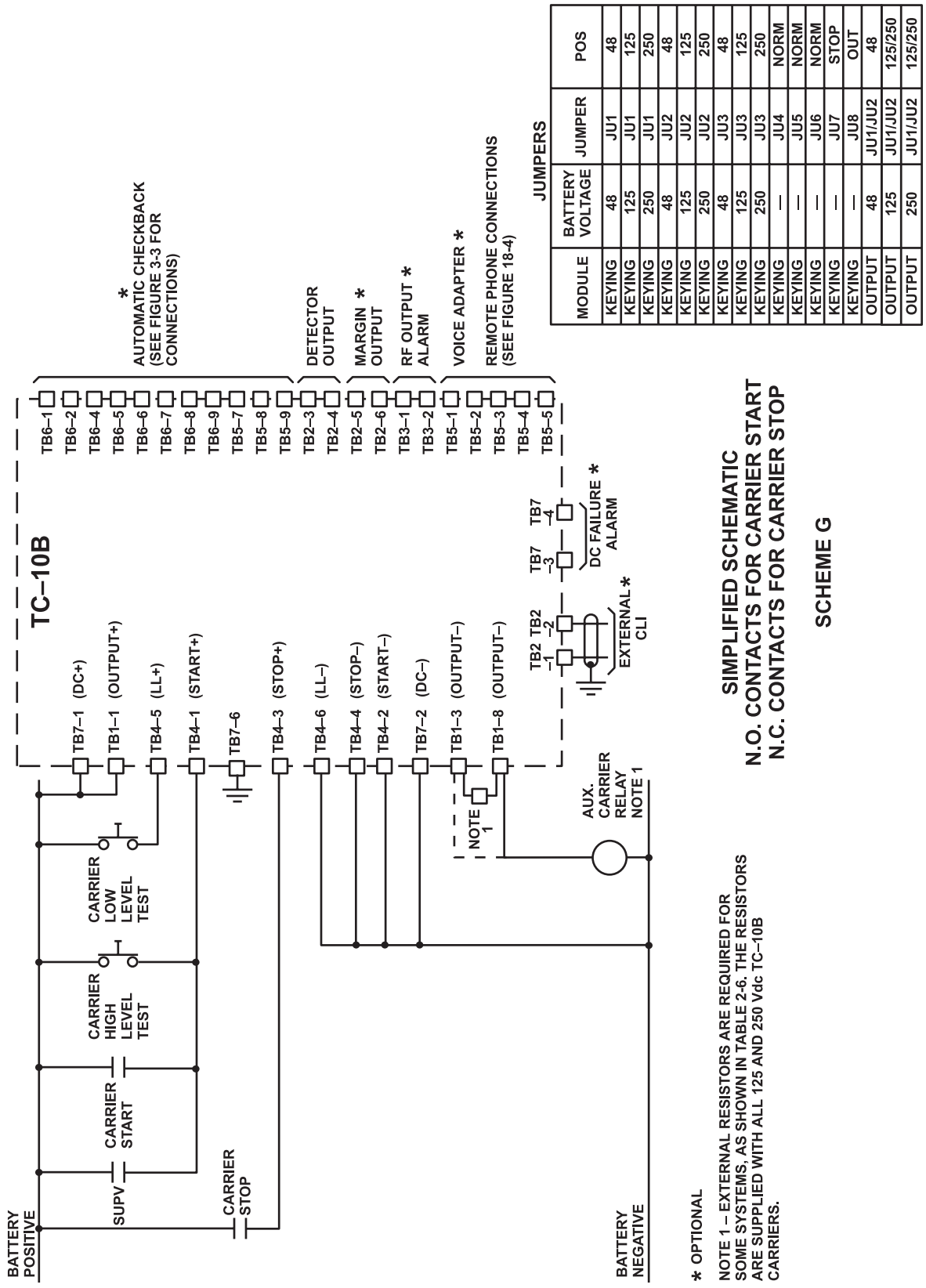
Figure 2–9. TC–10B Simplified Application Schematic – Scheme E (7833C63).



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	INV
KEYING	—	JU5	INV
KEYING	—	JU6	INV
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

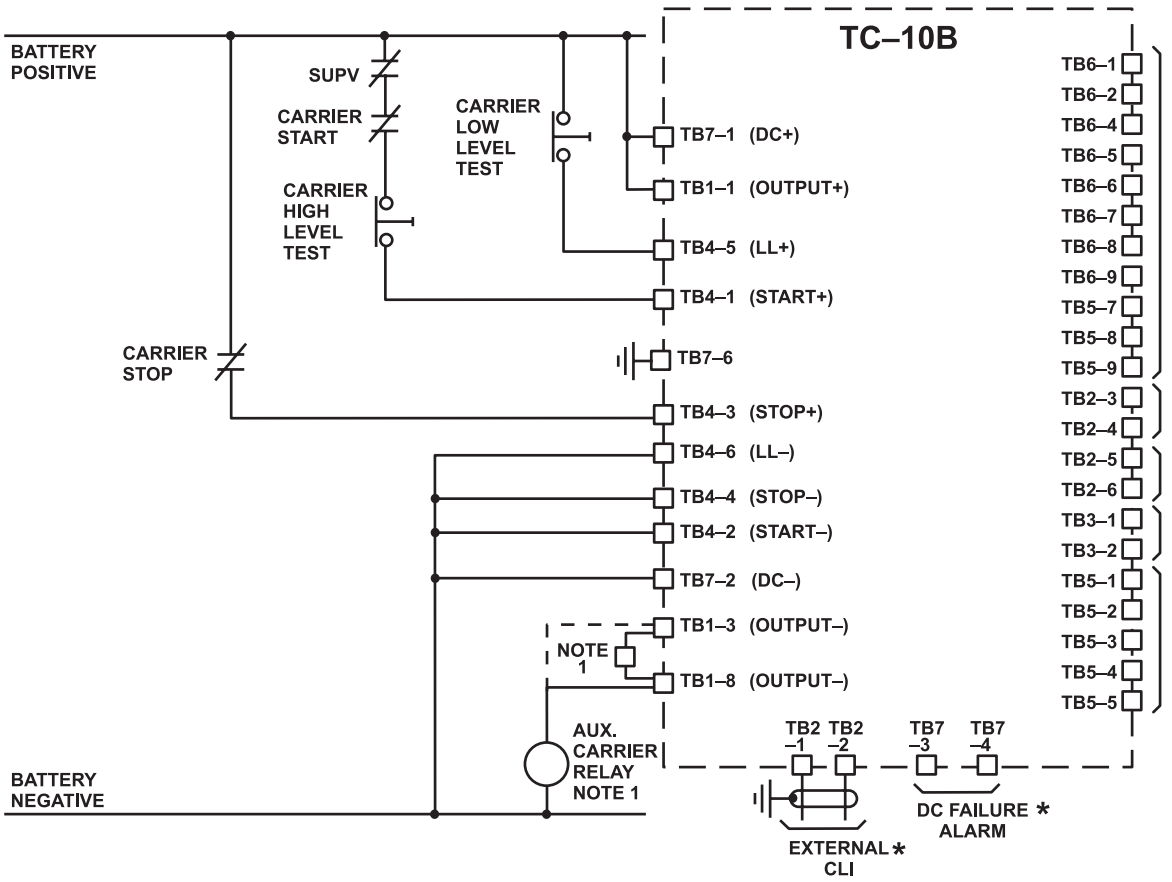
Figure 2–10. TC–10B Simplified Application Schematic – Scheme F (7833C63).



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	NORM
KEYING	—	JU5	NORM
KEYING	—	JU6	NORM
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

Figure 2–11. TC–10B Simplified Application Schematic – Scheme G (7833C63).



* OPTIONAL

NOTE 1 – EXTERNAL RESISTORS ARE REQUIRED FOR SOME SYSTEMS, AS SHOWN IN TABLE 2-6. THE RESISTORS ARE SUPPLIED WITH ALL 125 AND 250 Vdc TC–10B CARRIERS.

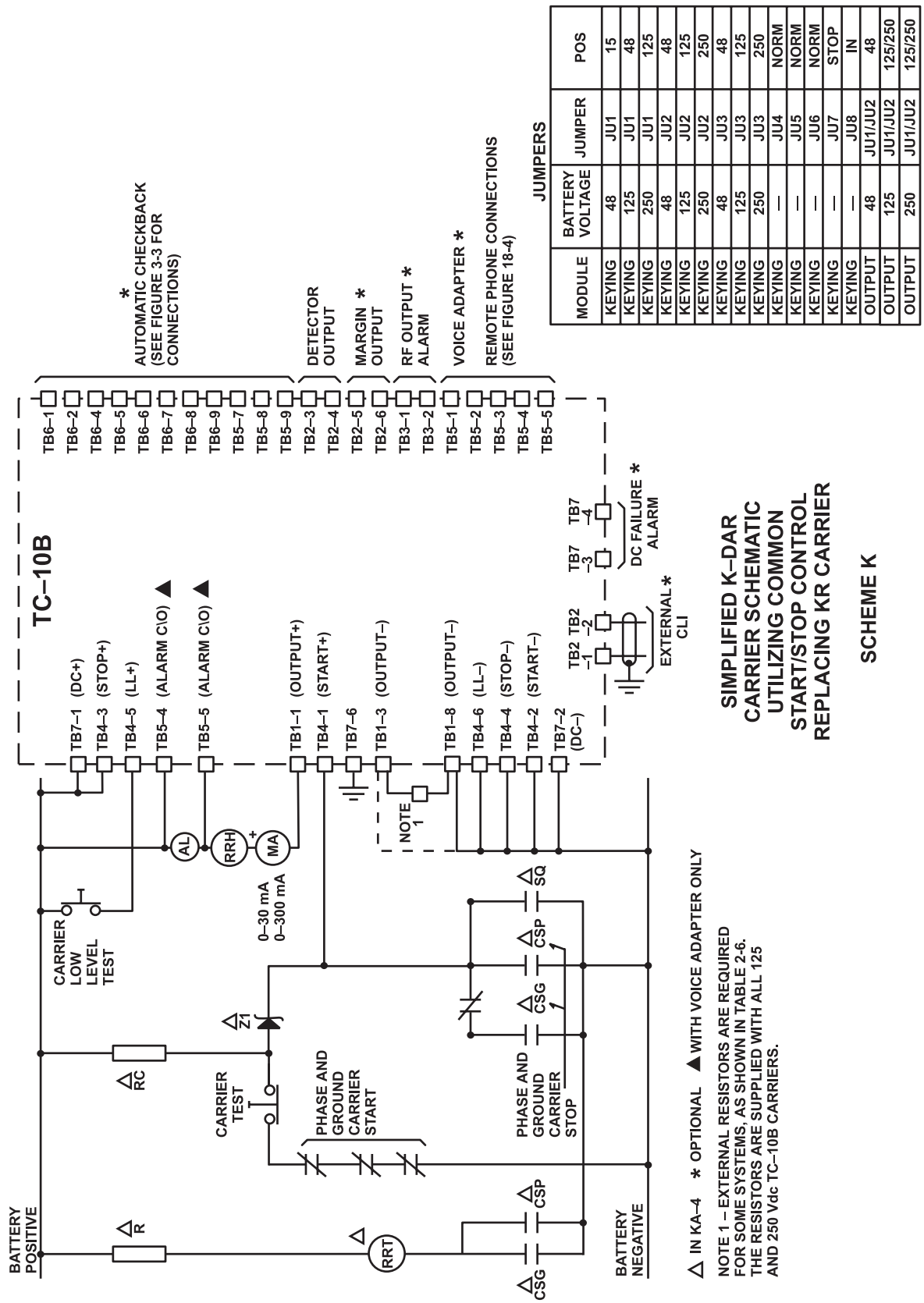
SIMPLIFIED SCHEMATIC
N.C. CONTACTS FOR CARRIER START
N.O. CONTACTS FOR CARRIER STOP

SCHEME H

JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	INV
KEYING	—	JU5	NORM
KEYING	—	JU6	INV
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

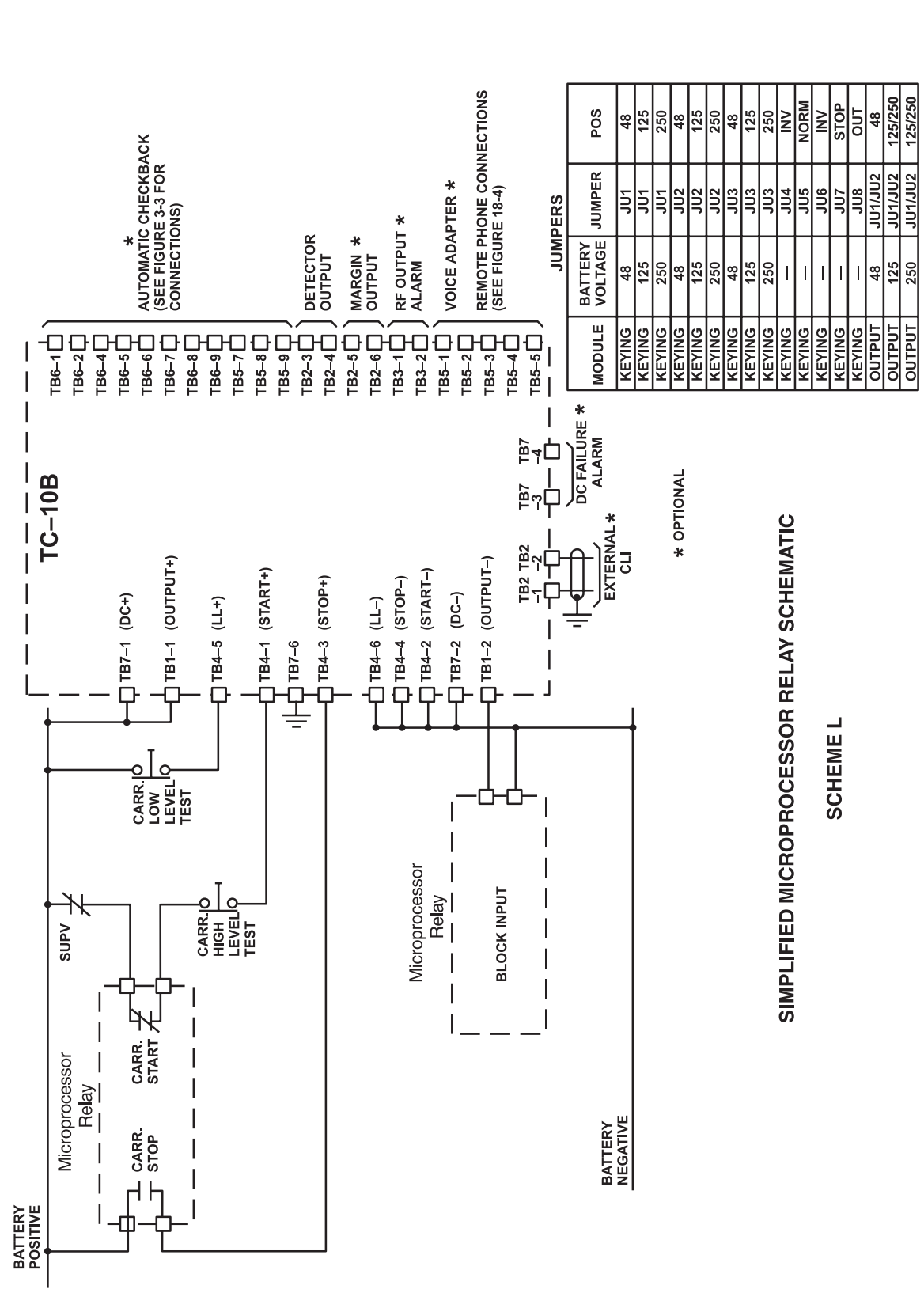
Figure 2–12. TC–10B Simplified Application Schematic – Scheme H (7833C63).



JUMPERS

MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	15
KEYING	125	JU1	48
KEYING	250	JU1	125
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	NORM
KEYING	—	JU5	NORM
KEYING	—	JU6	NORM
KEYING	—	JU7	STOP
KEYING	—	JU8	IN
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

Figure 2–13. TC–10B Simplified Schematic – Scheme K (7833C63).



MODULE	BATTERY VOLTAGE	JUMPER	POS
KEYING	48	JU1	48
KEYING	125	JU1	125
KEYING	250	JU1	250
KEYING	48	JU2	48
KEYING	125	JU2	125
KEYING	250	JU2	250
KEYING	48	JU3	48
KEYING	125	JU3	125
KEYING	250	JU3	250
KEYING	—	JU4	INV
KEYING	—	JU5	NORM
KEYING	—	JU6	INV
KEYING	—	JU7	STOP
KEYING	—	JU8	OUT
OUTPUT	48	JU1/JU2	48
OUTPUT	125	JU1/JU2	125/250
OUTPUT	250	JU1/JU2	125/250

Figure 2–14. TC–10B Simplified Applications Schematic – Scheme L (7833C63).

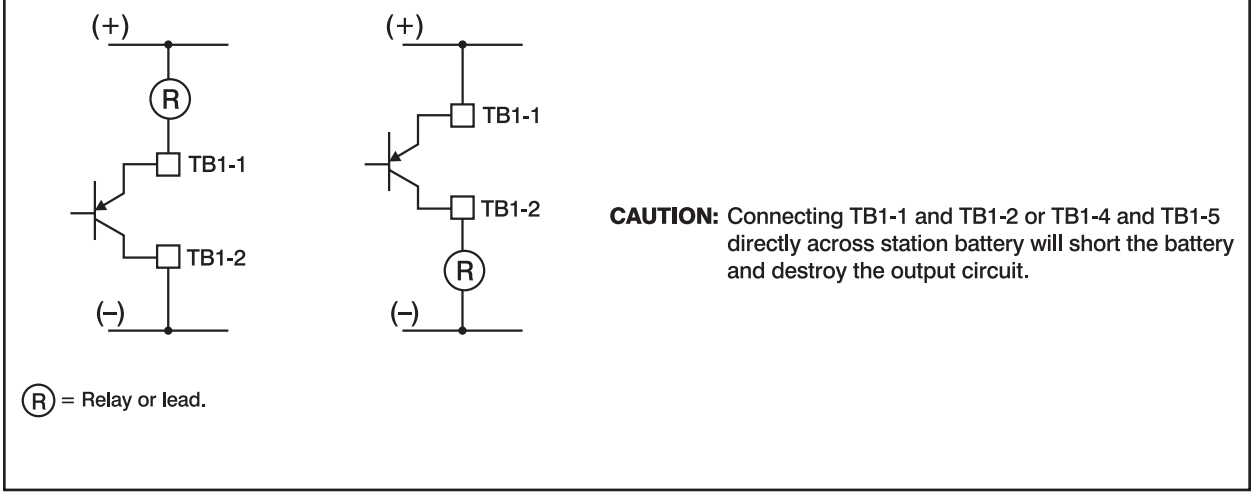


Figure 2–15. TC–10B Receiver Output Typical Connections.

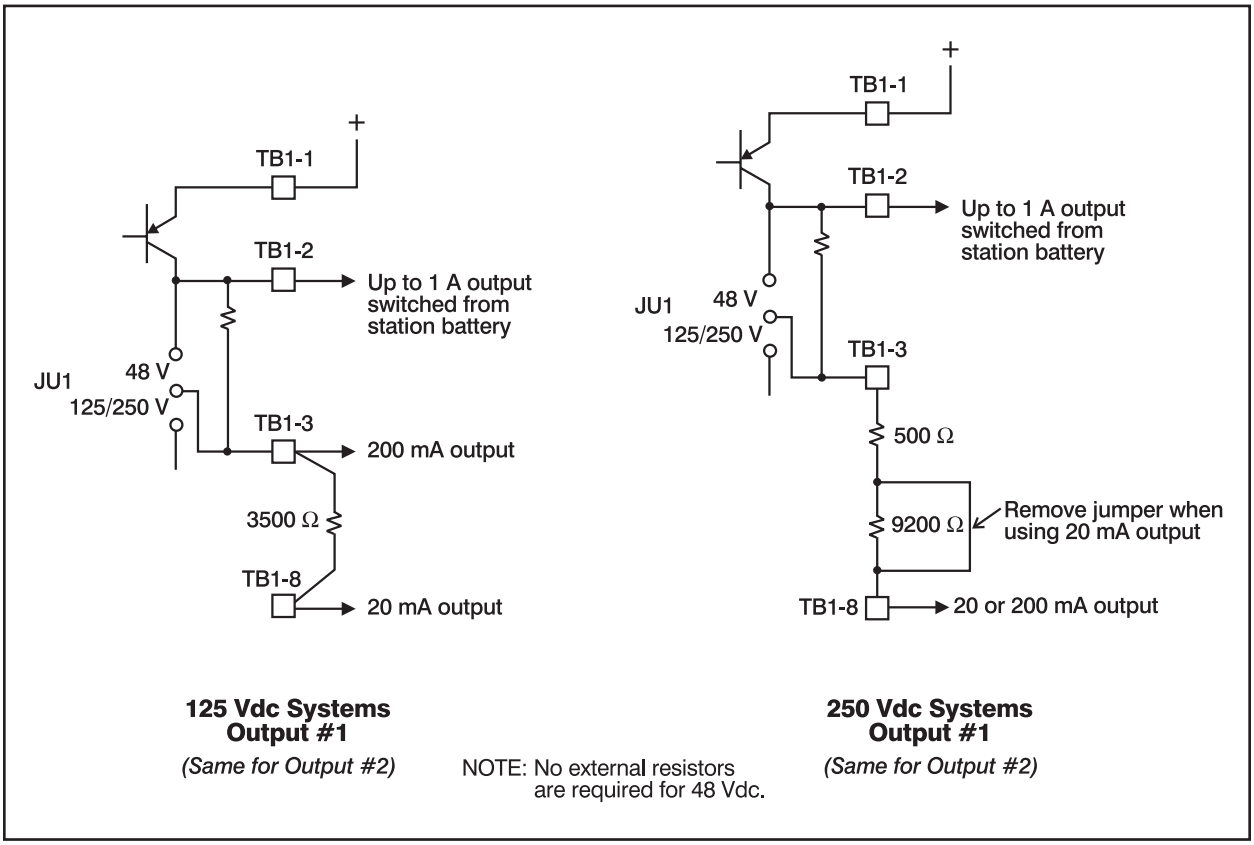


Figure 2–16. TC–10B Receiver Outputs with External Resistors — 125 Vdc and 250 Vdc Systems.

USER NOTES

Chapter 3. Installation

3.1 Unpacking

If the TC–10B is shipped unmounted, it is in special cartons that are designed to protect the equipment against damage.

⚠ CAUTION

UNPACK EACH PIECE OF EQUIPMENT CAREFULLY SO THAT NO PARTS ARE LOST. INSPECT THE CONDITION OF THE TC-10B AS IT IS REMOVED FROM ITS CARTONS. ANY DAMAGE TO THE TC-10B MUST BE REPORTED TO THE CARRIER. DAMAGES ARE THE RESPONSIBILITY OF THE CARRIER AND ALL DAMAGE CLAIMS ARE MADE GOOD BY THE CARRIER. SEND A COPY OF ANY CLAIM TO PULSAR TECHNOLOGIES, INC.

3.2 Storage

If you are setting the equipment aside before use, be sure to store it in its special cartons (in a moisture-free area) away from dust and other foreign matter.

3.3 Installation Location

Install the TC–10B in an area which is free from:

- Temperature exceeding environmental limits (See "Environmental Requirements" in Chapter 1)
- Corrosive fumes
- Dust
- Vibration

3.4 Assembly

You can assemble the TC–10B for use in any of the following configurations:

- Mounted in a fixed-rack cabinet.
- Mounted in a swing-rack cabinet
- Mounted on an open rack.

or in your own, customer-specified configuration. Refer to Figure 3-3 for mounting dimensions.

⚠ CAUTION

IF YOU ARE USING THE TC-10B WITH A SWING-RACK CABINET, MAKE SURE THAT THE CABINET IS FIRMLY FASTENED BEFORE OPENING THE RACK (TO PREVENT TIPPING).

3.5 TC–10B Rear Panel Connectors

The following connectors are accessible from the Rear Panel (See Figure 3-1):

- Terminal Blocks.
- Cable Jacks
- Jumpers
- Input/Output Pins

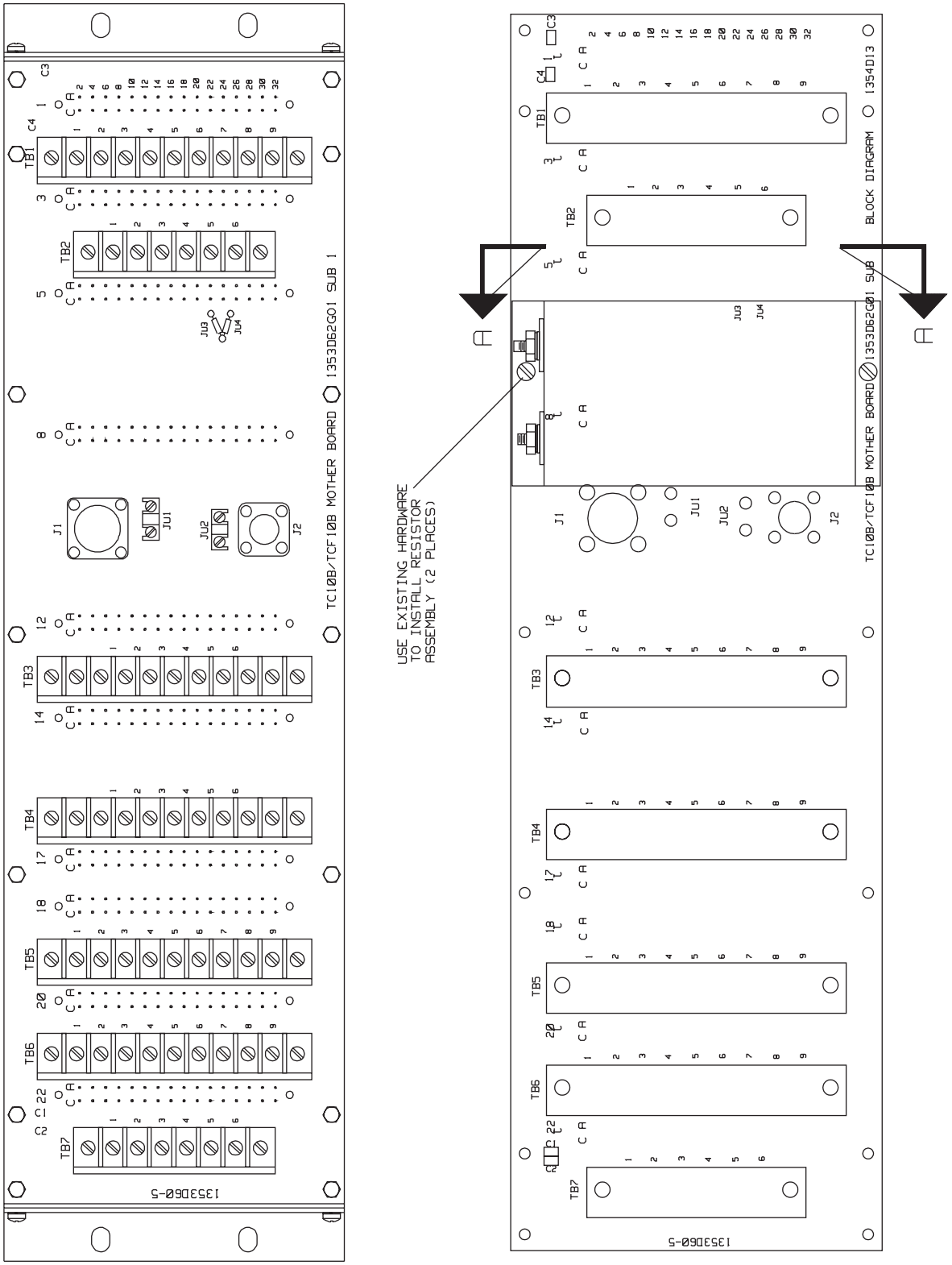


Figure 3–1. TC–10B Rear Panel – Mother Board (1354D16-12/1355D01).

3.5.1 Terminal Blocks

(Refer to Figure 3-4 for further explanation.)

TB7 Power Supply	(Terminals 1 thru 6)
TB6 Automatic Checkback	(Terminals 1 thru 9)
TB5 Voice Adapter	(Terminals 1 thru 9)
TB4 Keying	(Terminals 1 thru 6)
TB3 10W PA	(Terminals 1 thru 6)
TB2 Level Detector	(Terminals 1 thru 6)
TB1 Receiver Output	(Terminals 1 thru 9)

3.5.2 Cable Jacks

J1 RF Interface Module Transmitter, RF output line, thru 2-wire coaxial cable (UHF)

J2 RF Interface Module Receiver, RF input line thru 5,000 ohm 4-wire coaxial cable (BNC)

3.5.3 Jumpers

JU1 UHF Chassis Ground (for J1)

JU2 BNC Chassis Ground (for J2)

JU3 5.02 MHz signal for optional Voice Adapter

JU4 20 kHz signal for optional Voice Adapter

3.5.4 Input/Output Pins of Modules

Pins labeled C and A provide 16 input/output connections per module (using even numbers 2 through 32 for all modules) as follows:

- Power Supply (pins are to the right of TB7)
- Automatic Checkback (pins are to the right of TB6)
- Voice Adapter (pins are to the right of TB5)
- Keying (pins are to the left of TB4)
- Transmitter (pins are to the left of TB3)
- 10W PA (pins are to the right of TB3)
- RF Interface (pins are to the right of cable jacks and jumpers)
- Receiver (pins are to the left of TB2)
- Level Detector (pins are to the left of TB1)
- Receiver Output (pins are to the right of TB1)

3.6 Connections

3.6.1 Safety Precautions

Read this Installation chapter thoroughly before making any connections to the TC–10B. ***No one should be permitted to handle any of the equipment that is supplied with high voltage, or connect any external apparatus to the equipment, unless that person is thoroughly familiar with the hazards involved.***

Three types of connections are made:

- TC–10B equipment ground
- DC power supply and other connections
- Coaxial cables

⚠ CAUTION

PRIOR TO MAKING CONNECTIONS, CLOSE THE RF GROUNDING KNIFE SWITCH IN THE CABINET THAT IS CONNECTED TO THE INCOMING COAXIAL CABLE.

3.6.2 TC–10B Equipment Ground

In addition to the TC–10B chassis ground connection that is made through the cabinet or rack, a ground connection is provided at the Rear Panel Terminal Block TB7. (See Figure 3-1.) A connection should be made between TB7 Terminal 6 and the earth ground connection at the TC–10B cabinet location.

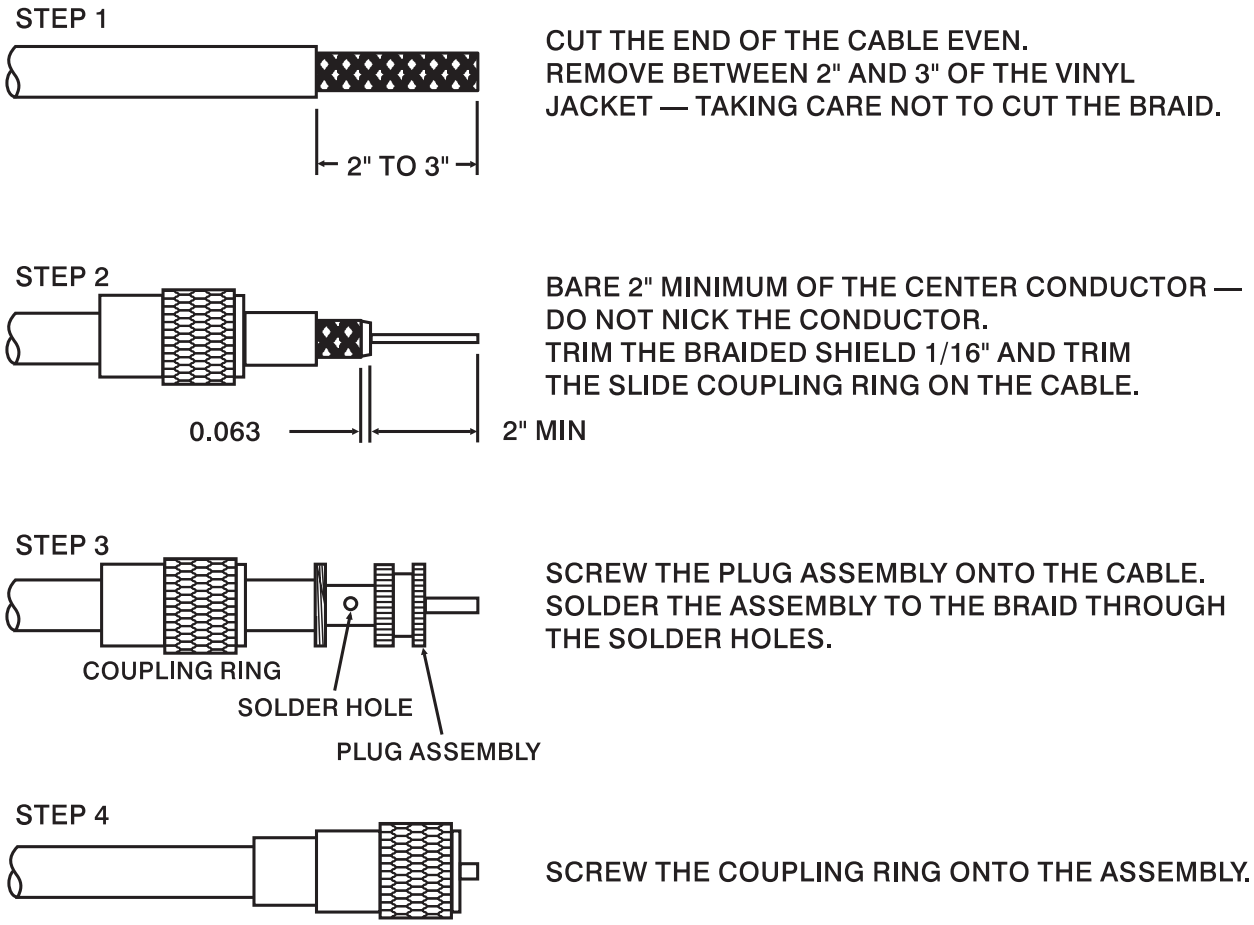


Figure 3–2. Cable Termination Diagram (9651A13).

3.6.3 DC Power Supply and Other Connections

Input terminals TB7-1 and TB7-2, on the rear of the TC–10B chassis, provide the connection points for the power supply (48, 125 and 250 Vdc) and customer interconnections. (See Figure 3-1.)

Any lead coming to or from the switchyard should be shielded twisted pair to reduce transients to below the Surge Withstand Capability of ANSI C37.90.1.

3.6.4 Coaxial Cable

A coaxial cable is required for a low-impedance path between the TC–10B (Transmitter and Receiver modules) and the Line Tuner (in the switchyard). Connection jack J1, on the Rear Panel, provides the point for coaxial cable connection from the TC–10B to the switchyard.

NOTE

The type of coaxial cable we recommend is RG-213/U (52 OHMS, 29.5 PF/FOOT) with the following characteristics:

- Single-conductor
- #12 AWG
- 7 strand #21 copper.
- Polyethylene insulator
- Copper shield
- Vinyl jacket (nominal O.D. 0.405 inch)

If the coaxial cable is to connect to related cabinets enroute to the switchyard, we recommend RG-58A/U cable from J1 to the related cabinets and RG-213/U from the cabinets to the switchyard. Install the coaxial cable according to the following guidelines:

1. Attach both ends of the coaxial cable in accordance with the Cable Termination Diagram (see Figure 3-2, terminal block lugs, as required).
2. To hold carrier loss to a minimum, keep the cable the shortest possible length.

   The minimum cable bending diameter is six times the cable diameter.
3. The copper braid of the cable must be grounded at the end which connects to the TC–10B.

⚠ CAUTION

DO NOT GROUND TO THE END OF THE CABLE THAT IS CONNECTED TO THE LINE TUNER.

4. Without grounding the copper braid of the cable, connect the cable to the ground terminal of the Line Tuner, at either of the following:
   - Impedance Matching Transformer
   - Wideband Filter

   If you are connecting the cable directly to the line tuner, the cable connector can enter the line tuner base either through the side or the bottom of the base.

3.7 Disconnections

⚠ CAUTION

NEVER DISCONNECT THE CARRIER LEAD-IN BETWEEN THE LINE TUNER AND THE COUPLING CAPACITOR UNLESS THE LOW POTENTIAL END OF THE COUPLING CAPACITOR IS GROUNDED.

BEFORE DISCONNECTING THE CARRIER LEAD-IN CONDUCTORS, CLOSE THE RF GROUNDING SWITCH AT THE BASE OF THE COUPLING CAPACITOR.

WARNING: IF THIS GROUND IS NOT PROVIDED, DANGEROUS VOLTAGES CAN BUILD UP BETWEEN THE LINE TUNER AND COUPLING CAPACITOR.

Table 3–1. Attenuator Override Jumper Sensitivity Levels.

	Normal Sensitivity		High Sensitivity	
	Wideband	Narrowband	Wideband	Narrowband
JU6 Position	OUT	OUT	IN	IN
Minimum Sensitivity (mV)	60	20	15	5
Maximum Input Level	70	70	17	17
Impedance (ohms)	5,000	5,000	1,000	1,000

3.8 Jumper Controls

Jumpers are set during installation, depending on the particular TC–10B features and applications (see Figure 3-5).

3.8.1 Power Supply PC Board

Jumper JU1 for optional Alarm Relay establishes contact type during loss of power condition (NO/NC).

> NOTE
>
> JU1 is shipped in the "NC" state.

3.8.2 Keying PC Board

For proper selection of jumpers, refer to Figures 2-5 through 2-14.

JU1 Carrier Start	15 V, 48 V, 125 V, 250 V
JU2 Carrier Stop	15 V, 48 V, 125 V, 250 V
JU3 Low-Level Key	15 V, 48 V, 125 V, 250 V
JU7 Carrier Start/ Stop Priority	START,STOP
JU6 Carrier Start	NORM (+), INVERT (-)
JU5 Carrier Stop	NORM (+), INVERT (-)
JU4 Low-Level Test	NORM (+), INVERT (-)
JU8 Carrier Stop	(KA-4, SKBU-1)

3.8.3 Transmitter PC Board

There are no jumpers on the Transmitter PC Board.

> NOTE
>
> JU1 is shipped in the "NC" state.

3.8.4 10W PA PC Board

Jumper JU1 for optional Alarm Relay establishes loss of power condition (NO/NC).

3.8.5 RF Interface PC Board

Matching Impedance Jumpers:

- JU4 50 ohms
- JU3 75 ohms
- JU2 100 ohms

2-wire or 4-wire RF Termination

- JU1/JU5 “IN” (2-wire)
- JU1/JU5 “OUT” (4-wire)

> NOTE
>
> JU1 is shipped in the “NC” state.

Attenuator Override Jumper (JU6)
(See Table 3-1.)

3.8.6 Receiver PC Board

Jumper JU1 should always be in the “NORM” position.

3.8.7 Level Detector and CLI PC Board

Jumper JU1 provides alternate contact status (NO/NC) for margin relay.

3.8.8 Receiver Output PC Board

Jumpers provide voltage selections as follows:

JU1

1. 48 V
2. 125/250 V

JU2

1. 48 V
2. 125/250 V

3.8.9 Master Checkback PC Boards

Refer to Chapter 17 (Automatic Checkback System) for proper jumper selection. The following jumpers are provided on the Master Checkback Module:

JU1–JU6 Test Sequence

JU7 Clock Frequencies and Transmission Rates

JU8 Checkback Waiting (Response) Interval

JU9 Retry on Failure

JU10 Checkback Interval Timer

JU11 Stop after Failure

JU12 Alarm (Momentary/Seal-in)

JU13 Optional Events Counter

JU14 Auto Initiate (Block on Fail/Normal)

JU15 Supervisory Control Initiate

3.8.10 Remote Checkback PC Board

Refer to Chapter 17 for proper jumper selection. The following jumpers are provided on the Remote Checkback Module:

JU1 Remote Module Number

JU2 Daisy Chain or Normal

JU3 Supervisor Control Initiate

JU4 Voltage Level for Daisy Chain

JU5 Clock Frequencies and Transmission Rates

3.8.11 Voice Adapter PC Board

Four jumpers are provided, as follows:

JU1 Receiver Squelch (IN/OUT)

When the jumper is “IN”, voice keying squelches the receive audio signal.

JU2/
JU3 Compandor (IN/OUT)

When the jumper is “IN”, the audio is compandored; when the jumper is “OUT”, the audio is not compandored.

JU4 Signalling (TC/TCF)

When jumper is set for “TC”, and handset is plugged into handset jack, the alarm Cutoff from the handset jack will cause the relay to operate. When jumper is set for “TCF”, the presence of a signaling tone will operate the relay.

JU5 Alarm Contacts (NO/NC)

When jumper is set in “NO” position, and relay is de-energized, the alarm contacts will be “OPEN”. When jumper is in “NC” position, and relay is de-energized, the alarm contacts will be “CLOSED”.

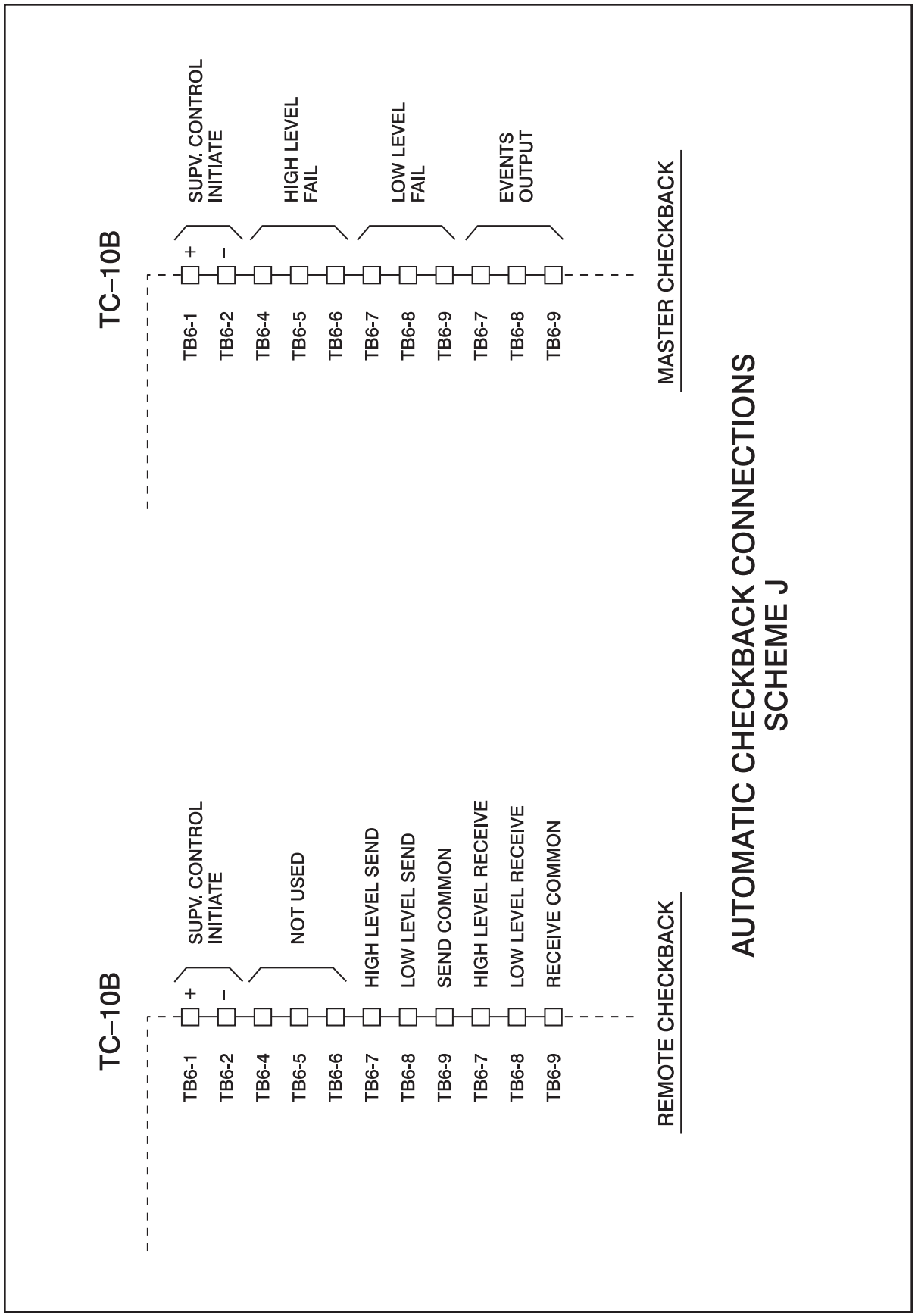


Figure 3–3. TC–10B Simplified Application Schematic (Scheme J). (7833C63)

USER NOTES

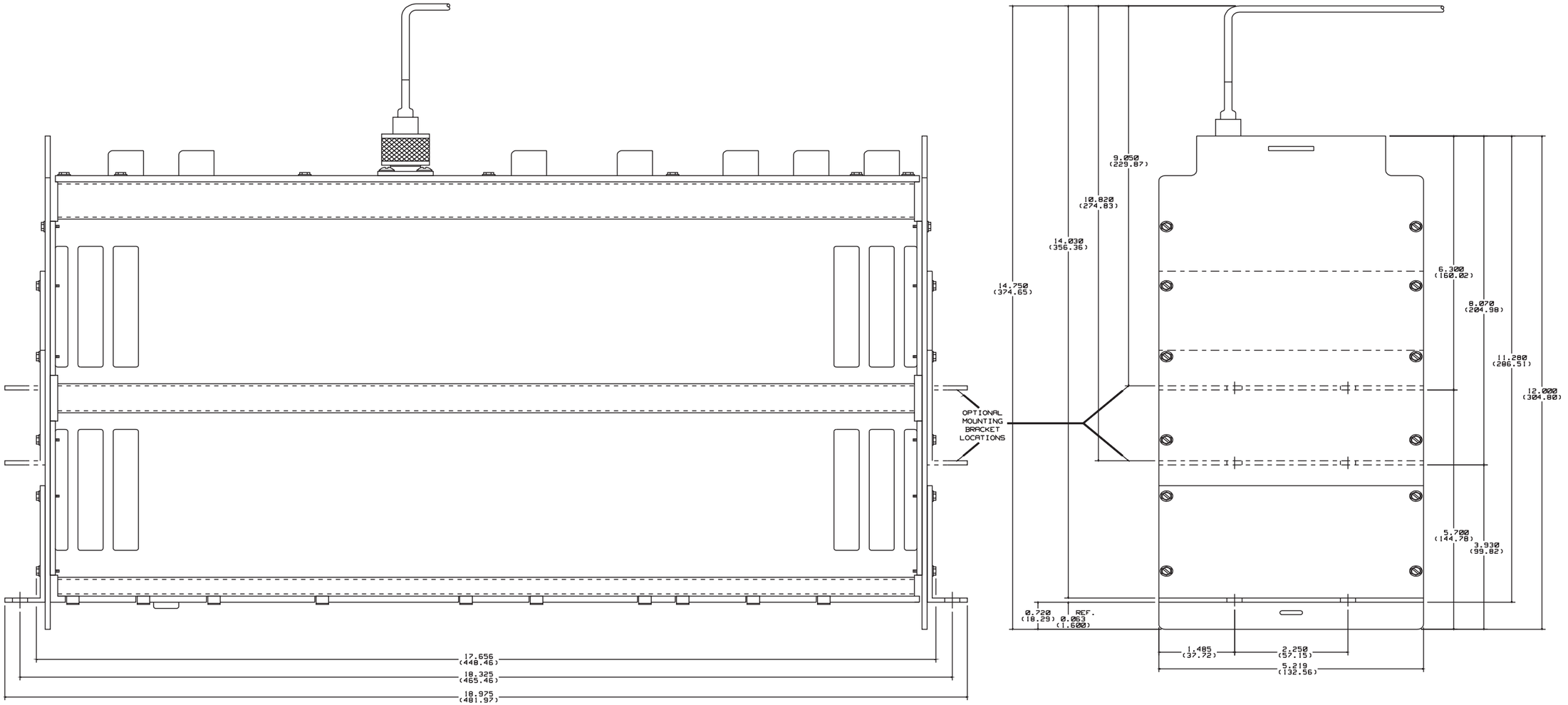
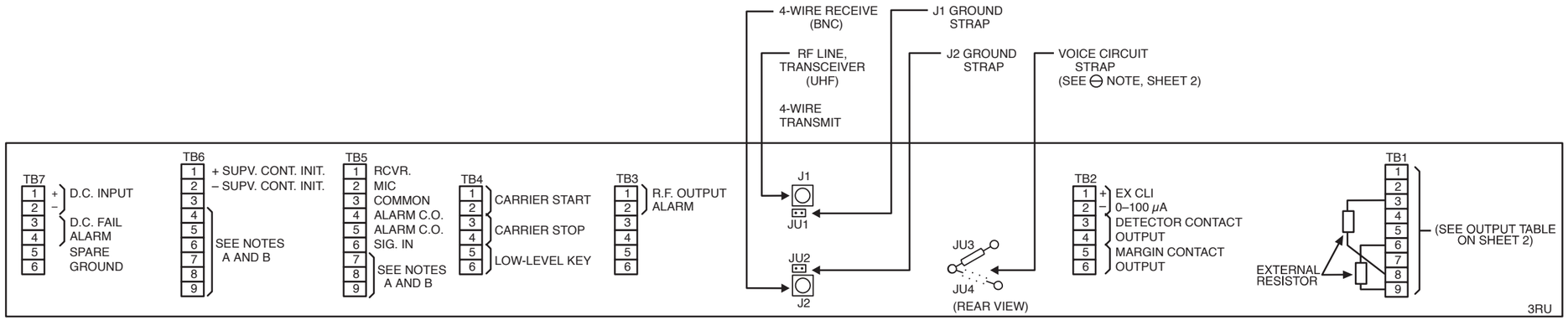
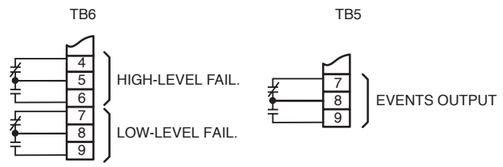


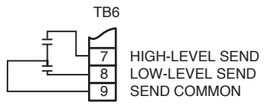
Figure 3–4. TC–10B/TCF–10B Mechanical Outline Drawing (1354D48).



NOTE A – MASTER CHECKBACK OUTPUTS (WHEN USED)



NOTE B – REMOTE CHECKBACK DAISY CHAIN OUTPUTS (WHEN USED)



– REMOTE CHECKBACK DAISY CHAIN INTPUTS (WHEN USED)

OPTIONS

ALARM & CLI
- D.C. FAILURE ALARM
- R.F. OUTPUT ALARM RELAY
- CARRIER LEVEL MARGIN ALARM RELAY
- CLI ON MODULE AND ANALOG OUTPUT (0–100 μA)

VOICE – VOICE ADAPTER MODULE

JUMPER OPTIONS

POWER SUPPLY

JU1 NORMALLY OPEN/ NORMALLY CLOSED ALARM CONTACT

CHECKBACK

SEE INDIVIDUAL MODULE INSTRUCTIONS

VOICE

JU1 IN/OUT FOR SQUELCH
JU2 IN/OUT FOR COMPRESSOR
JU3 IN/OUT FOR EXPANDER
JU4 TC/TCF
JU5 NO/NC FOR ALARM

KEYING MODULE

JU1 *CARRIER START
JU2 *CARRIER STOP
JU3 *LOW-LEVEL
JU4 **LOW-LEVEL
JU5 **STOP
JU6 **START
JU7 FOR TEST PURPOSES ONLY
JU8 FOR USE WITH KA-4 AND SKBU-1

* EACH MUST BE STRAPPED FOR CORRECT VOLTAGE. REFER TO JUMPER TABLE IN FIGURES 2-5, 2-6, AND 2-7 (SIMPLIFIED SCHEMATICS) FOR TYPICAL APPLICATIONS.

** SELECTS SENSE OF INPUT DESIRE (NORMAL/INVERT).

POWER AMPLIFIER

JU1 NORMALLY OPEN/ NORMALLY CLOSED CONTACT OUTPUT

RF INTERFACE

JU1 IN 2-WIRE; OUT 4-WIRE
JU2 IMPEDANCE – 100 OHM
JU3 IMPEDANCE – 75 OHM
JU4 IMPEDANCE – 50 OHM
JU5 IN 2-WIRE; OUT 4-WIRE
JU6 NORM/HIGH SENSITIVITY

CLI DETECTOR

JU1 NORMALLY OPEN/ NORMALLY CLOSED CONTACT OUTPUT

OUTPUT BOARD

JU1 48 OR 125/250 V
JU2 48 OR 125/250 V

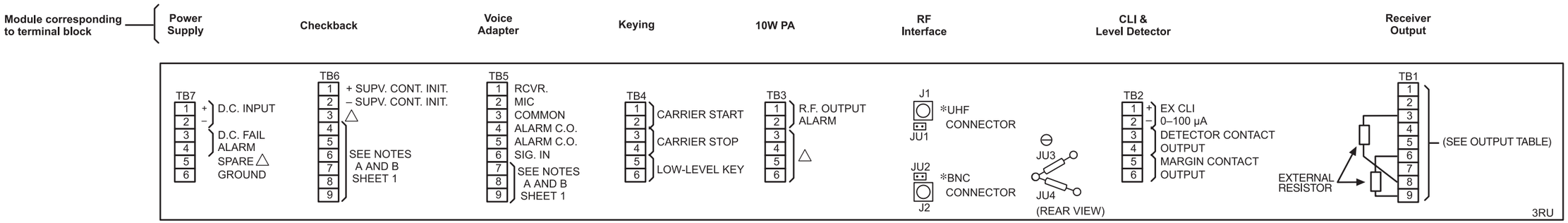
RECEIVER

JU1 NORMAL OR DISABLE OF RECEIVER

Figure 3–5. TC–10B Connection Drawing and Jumper Options (2064D87; Sheet 1 of 2).

TC-10B CHASSIS WIRING BREAKDOWN

(Shows which terminals are wired for different catalog number options.)



Chassis Options	Module Options		Terminal Blocks Used
Only offered as a transceiver (transmitter and receiver)	1. None (basic transceiver)		TB1 (1–9), TB2 (3, 4), TB4 (1–6), TB7 (1, 2, 6)
	2. Voice adapter		TB5 (1–6)
	3. Alarms/CLI (includes DC fail, R.F. output alarm, margin contact, and external CLI output)		TB2 (1, 2, 5, 6) TB3 (1, 2) TB7 (3, 4)
	4. Checkback	A. Master	TB6 (1, 2, 4–9); TB5 (7–9)
		B. Remote (no daisy chain)	TB6 (1, 2)
		C. Remote (with daisy chain)	TB6 (1, 2, 7–9); TB5 (7–9)

✻ – J1 and J2 coaxial connectors may be wired out to terminal blocks or connected to RF hybrids. J1 is used for either the 2-wire transceiver output or the 4-wire transmitter output. J2 is used for the 4-wire receive input only.

△ – These terminals do not need to be wired out.

⊖ – Jumper is always in position JU3. (JU3 applies a 5-MHz signal to the voice adapter.)

OUTPUT TABLE

For use with Microprocessor-based Relays

1 Amp Switched Transistor Output	Terminal Connections OUTPUT #1		Terminal Connections OUTPUT #2	
	TB1-1 & TB1-2		TB1-4 & TB1-5	

For use with Electro-Mechanical Relay Systems

Carrier Aux Relay	Battery Voltage (Vdc)	External Resistor (ohms/watts)	Terminal Connections OUTPUT #1	JU1 Position	Terminal Connections OUTPUT #2	JU2 Position
20 mA (2200 Ω)	48	None required	TB1-1 (+) & TB1-3	48	TB1-4 (+) & TB1-6	48
20 mA (2200 Ω)	125	3500/5	TB1-1 (+) & TB1-8	125/250	TB1-4 (+) & TB1-9	125/250
20 mA (2200 Ω)	250	9200/10 & 500/40	TB1-1 (+) & TB1-8	125/250	TB1-4 (+) & TB1-9	125/250
200 mA (25 Ω)	48	None required	TB1-1 (+) & TB1-3	48	TB1-4 (+) & TB1-6	48
200 mA (25 Ω)	125	None required	TB1-1 (+) & TB1-3	125/250	TB1-4 (+) & TB1-6	125/250
200 mA (25 Ω)	250	500/40	TB1-1 (+) & TB1-8	125/250	TB1-4 (+) & TB1-9	125/250

Figure 3–6. TC–10B Connection Drawing and Jumper Options (2062D38; Sheet 2 of 2).

Chapter 4. Test Equipment

Table 4-1 shows the equipment you should use to perform the Acceptance Tests (Chapter 5) and Routine Adjustments (Chapter 6).

Table 4–1. Recommended Test Equipment.

Equipment	Application
High-Impedance Selective Level Meter, 300 Hz to 1 MHz (Rycom 6021A)*	• Impedance Matching • Transmitter Power Adjustment • Receiver Margin Setting
Current Meter (Simpson 260)*	Check dc Supply
Reflected Power Meter, Auto VLF Power SWR Meter (Signal Crafter 70)*	Impedance Matching at Carrier Output
Oscilloscope (Tektronix)*	• Transmitter Power • Adjustment for Optional Voice Adapter Module
Frequency Counter, 80 MHz (H/P5381A)*	• Transmitter Frequency • Offset for three-terminal line applications
Non-Inductive Resistor, 50 Ohm, 25 W (Pacific)*	Transmitter Termination
Signal Generator (H/P 3325A)*	General ac output for lab measurements
Extender Board (1353D70G01)	(See Figure 4-1.)
Current monitoring cord (Pomona Electronics 2977-J-36)*	Used with standard telephone jack.

⚠ CAUTION

WE RECOMMEND THAT THE USER OF THIS EQUIPMENT BECOME THOROUGHLY ACQUAINTED WITH THE INFORMATION IN THESE INSTRUCTIONS BEFORE ENERGIZING THE TC–10B AND ASSOCIATED ASSEMBLIES. YOU SHOULD NOT REMOVE OR INSERT PRINTED CIRCUIT MODULES WHILE THE TC–10B IS ENERGIZED. ALL INTEGRATED CIRCUITS USED ON THE MODULES ARE SENSITIVE TO AND CAN BE DAMAGED BY THE DISCHARGE OF STATIC ELECTRICITY. YOU SHOULD ALWAYS OBSERVE ELECTRO-STATIC DISCHARGE PRECAUTIONS WHEN HANDLING MODULES OR INDIVIDUAL COMPONENTS. FAILURE TO OBSERVE THESE PRECAUTIONS CAN RESULT IN COMPONENT DAMAGE.

* Indicates “or equivalent” of the recommended equipment item.

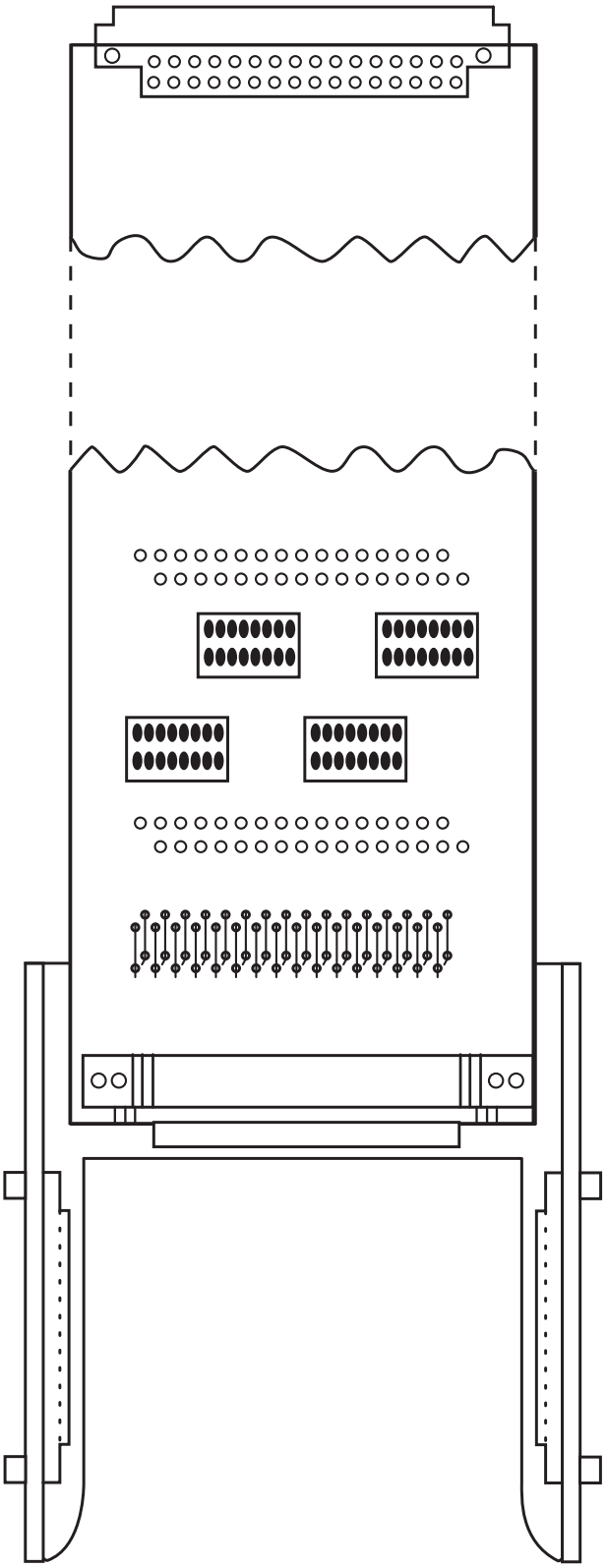


Figure 4–1. Extender Board.

Chapter 5. Acceptance Tests

You may perform the following TC–10B acceptance tests at your installation to determine compliance of the TC–10B with factory specifications. (See Test Equipment in Chapter 4 and Signal Path in Chapter 7.)

5.1 Preliminary Checks

5.1.1 Check Chassis Nameplate.

Verify that the proper dc supply voltage and module options are on the chassis nameplate.

Check to ensure that all required modules are supplied and are installed in the proper chassis slots. The slots are labeled on the top edge of the chassis.

5.1.2 Check for Bandpass Filter Type on Receiver Module

Check for wide or narrow bandpass filter (FL1) on the Receiver Module, as required (refer to Table 2-2 and Table 2-3):

- Wideband filter (1200 Hz standard) Style Number 1353D78H03
- Narrowband filter (600 Hz special) Style Number 1353D78H02

5.1.3 Inspecting for the Correct dc Voltage

With the power "OFF," remove the Power Supply Module and inspect it for the correct dc voltage, as specified in Table 5-1.

Table 5–1. Voltage Specifications.

Specified	Style # 1617C38GXX
48 V with Alarm Relay	G01
125 V with Alarm Relay	G02
250 V with Alarm Relay	G03
48 V w/o Alarm Relay	G04
125 V w/o Alarm Relay	G05
250 V w/o Alarm Relay	G06

5.2 Preliminary Settings

Before starting the test, set the jumpers on the various modules according to the instructions in the sections below.

5.2.1 Power Supply Module

JU1 N.C. (loss of power condition)

5.2.2 Keying Module

JU1 Set to dc supply voltage

JU2 Set to dc supply voltage

JU3 Set to dc supply voltage

JU4 NORM

JU6 NORM

JU7 NORM

JU8 OUT

5.2.3 Transmitter Module

Set the four rotary switches to 250 kHz or desired frequency.

5.2.4 10W PA Module

JU1 N.C. (loss of power condition)

5.2.5 RF Interface Module

Matching Impedance Jumper

JU4 (50 ohms)

2-Wire or 4-Wire RF Termination

JU1/JU5 (out, 4 wire)

Attenuator Override Jumper

JU6 (NORM Sensitivity)

5.2.6 Receiver Module

JUl Normal position

Set the rotary switches to 250 kHz or the desired frequency.

5.2.7 Level Detector Module

JUl N.O. (margin relay)

5.2.8 Receiver Output Module

JU1 Set to dc supply voltage

JU2 Set to dc supply voltage

5.2.9 Optional Checkback Module (if supplied)

Master Checkback (Trial Settings)

S2-	1	2	4	8	16	32	64	128	(C'back Interval)
	Dn	Up	Up	Up	Up	Up	Up	Up	
S5	A0	A1	A2	A3	A4				(Transmit Address)
	Dn	Up	Dn	Up	Dn				
S6	A0	A1	A2	A3	A4				(Receive Address)
	Dn	Up	Dn	Up	Dn				

JU1 A (LL1)

JU2 B (HLI)

JU3 C (LL2)

JU4 D (HL2)

JU5 E (LL3)

JU6 F (HL3)

JU7 A (Soldered on Main Board)
Normal 192 Hz

JU8 B (2 Sec Waiting Interval)

JU9 B (Retry on Failure .... Yes)

JU10 B (Checkback Interval .... Normal)

JU11 B (Stop at Failure .... No Stop)

JU12 B (Momentary Alarm)

JU13 I (Total Failures, if supplied)

JU14 B (Normal ... does not block on Fail)

Remote Checkback

JUl 1 (Remote #1)

JU2 A (Normal ... without daisy chaining)

JU3 Set to dc Supply Voltage

JU4 Set to dc Supply Voltage

JU5 A (Normal...384 Hz)

S2-	A0	A1	A2	A3	A4	(Transmit Address)
	Dn	Up	Up	Up	Up	
S5	A0	A1	A2	A3	A4	(Receive Address)
	Dn	Up	Dn	Up	Dn	

5.2.10 Optional Voice Adapter Module (if supplied)

JU1 IN

JU2 IN

JU3 IN

JU4 TC

JU5 N.C.

5.3 ELECTRICAL TESTS

1. Refer to Figure 3-4 or Figure 7-1 for keying and output connections.
2. Connect the dc supply to the appropriate terminals on the rear panel (see Figure 3-4 or Figure 7-1).

⚠ CAUTION

ALWAYS TURN "OFF' dc POWER WHENEVER REMOVING OR INSTALLING MODULES.

3. Terminate the Transmitter output with a noninductive 50 ohm, 10 W resistor.
4. Connect the Selective Level Meter (Rycom 6021A) across the 50 ohm resistor load.
5. Allow a one-hour warm-up period before making the final frequency adjustments.

5.3.1 Power Supply Module Tests

1. Remove all modules except for the Power Supply Module.
2. Turn "ON" the dc power; measure the dc voltage at the Power Supply test jacks with the meter reference connected to TJ2:
   - TJ1/TJ2 (+20 Vdc ± 1 Vdc).
   - TJ3/TJ2 (-20 Vdc ± 1 Vdc).

NOTE

Prolonged operation with no load can cause the power supply to shut down (see Chapter 9, Section 9.2.2).

3. Turn "OFF" the dc power. Insert all modules into their appropriate slots in the chassis.
4. Repeat Step 2 (above). Both LEDs (D3, Input, and Dl1, Output) on the Power Supply Module must be "ON".
5. Place the current meter (Simpson 260 or equivalent) in series with the dc supply, and check the standby (unkeyed) current for the appropriate voltage source, as follows:

VOLTAGE	CURRENT
48 Vdc	.6 to .8 Amps
125 Vdc	.4 to .6 Amps
250 Vdc	.1 to .2 Amps

5.3.2 Transmitter Module Tests

Levels

1. Using the appropriate voltage (15 V, 48 V, 125 V, or 250 V), key the carrier start and observe that the level across the 50 ohm load is approximately 10 W per Table 5-2.
2. Using the Keying Module pushbutton switches, key the Transmitter (XMTR) Module for low-level (LL/1 W) and high-level (HL/10 W) power, as shown in the table below. If the voltage across the 50 ohm load is not approximately equal to the value shown in Table 5-2, place the Transmitter (XMTR) Module on an extender board and make adjustments (using R13 for 10 W and R12 for 1 W, respectively).

Table 5–2. Voltage Levels.

Keyed Level	Volts Across 50 W Load (V rms)	XMTR Adjust	dBm REF
LL – 1 W	7.07	R13	+30 dBm
HL – 10 W	22.4	R12	+40 dBm

3. Using the keying inputs on the rear of the chassis, key the Transmitter using the combinations listed below. Observe the output levels and logic per Table 5-3 below:

Keying Logic

Table 5–3. Keying Logic.

	Low-Level Start	High-Level Start	Stop	Output
(1)	ON			1 W
(2)	ON		ON	NONE
(3)		ON		10 W
(4)		ON	ON	NONE

NOTE

You can key low-level by placing the appropriate voltage (15 V, 48 V, 125 V, or 250 V) across TB4, pins 5 and 6, on the rear panel. You can key high-level start by placing the voltage across TB4, pins 1 and 2. You can key carrier stop by placing the voltage across TB4, pins 3 and 4.

5.3.3 Receiver Module Tests

Preliminary Steps

1. Remove the Keying Module from the chassis.
2. Connect the RF Signal Generator (H/P 3325A) to the UHF Chassis RF input jack (J1 on the rear panel.
3. On the RF Interface Module, reset jumpers JU1 and JU5 to “IN”.

Received Signal Path

1. Set the Signal Generator to 250 kHz, at a level of 1.0 V rms.

NOTE

Measure the signal generator level with an external voltmeter.

2. Measure the input signal level at the Receiver Front Panel (INPUT, COM test jacks); the level should be between 150 and 250 mV rms.

NOTE

Do not use coaxial cable for this measurement.

3. Disconnect the Signal Generator (from J1) and connect it to the chassis at BNC RF input jack (J2) on the rear panel.
4. Measure the input signal level at the Receiver (INPUT, COM test jacks); the level should be between 180 and 260 mV rms.

Receiver Sensitivity

1. Place the Receiver Module on an Extender Card (see Figure 4-1); then set the Receiver at 535.0 kHz.
2. Set the Signal Generator to 535 kHz, at a level of:
   - 60 mV rms (wideband–1353D78H03 Filter)
   - 20 mV rms (narrowband–1353D78H02 Filter)
3. Set the Level Adjust Attenuator (R3) on the Receiver Module to full CW.
4. Monitor the 20 kHz output (connector pins 28A to 32 C/A)

NOTE

The 20 kHz IF must be within 20 Hz before you proceed with the following steps. Adjust the crystal oscillator (C68) on the Receiver Module, if necessary.

5. Adjust the IF Gain Control (R68) on the Receiver Module, for output level of 63 mVrms.

Table 5–4. Level Detector and CLI Test Procedure Specifications.

Wide Band Receiver Input Level (mV) rms	Narrow Band Receiver Input Level (mV) rms	Adjusting Potentiometer	LEDs	CLI Reading (dB)
33.73	11.24	R29		-20
60.00	20.00	R18	DETECT	-15
106.00	35.30		DETECT	-10
190.00	63.30		DETECT	- 5
337.00	112.20	R23	MARGIN,DETECT	0
600.00	200.00		MARGIN,DETECT	+5
1060.00	353.00	R38,61	MARGIN,DETECT	+10

NOTE

If you cannot reduce output to this level using R68, adjust the attenuator (R3) on the Receiver Module until you can obtain 63 mV rms.

6. Reset the Signal Generator and Receiver Module to 250 kHz at 20/60 (narrowband/wideband) mV rms and verify that the 20 kHz output at connector pin 28-A is at least 63 mV rms. Using R3 on the front of the Receiver Module, reduce the 20 kHz level at pin 28-A to 63 mV rms.

5.3.4 Level Detector and CLI Module Tests

Preliminary Steps

1. Connect the RF Signal Generator (H/P 3325A) to the chassis at the BNC RF input jack (J2) on the "Motherboard."
2. Set the Synthesizer dials (on Receiver) to 250 kHz.

Level Detector and CLI Test Procedure

1. Set the Signal Generator to 250 kHz.
2. All CLI Meters (Internal and/or External) should read within ±2 dB of the specified readings, and within ±2 dB of each other (see Table 5-4).

NOTE

Margin and detect LEDs on the Level Detector Module should light as indicated in Table 5-4. (*should just light at this level.) The input signal is measured at the signal generator output. Adjust the specified potentiometers on the Level Detector Module if required.

3. Disconnect the RF Signal Generator from the Motherboard jack (J2).

5.3.5 Receiver Output Module Tests

Preliminary Steps

1. Connect a power supply source (48, 125, or 250 Vdc) to the following Rear Panel terminals (with reference to TB7-2):
   - Receiver Output #1: TB1-1 (+)
   - Receiver Output #2: TB1-4 (+)
2. Connect the Signal Generator (H/P 3325A) to the chassis at the UHF RF Input jack (J1) on the rear panel.

3. Place the Receiver Output Module on an Extender Board (see Figure 4-1).

Receiver Output Test Procedure

1. Set the Signal Generator to 250 kHz, at a level between 150 and 250 mV rms (The DETECT LED should be on.)
2. Measure the voltage level at TB1-2 with TB7-2 as a reference. This voltage should be the same as the power supply source (48, 125, or 250 Vdc). Also, measure the voltage level at TB1-5 with TB7-2 as a reference. This should be the same as the power supply source (48, 125, or 250 Vdc).
3. Remove the input signal, ensuring that the output level drops out.
4. Load down the output by connecting the appropriate resistor, as shown in Table 5-5.
5. Insert a current meter (Simpson 260 or equivalent) in the circuit by connecting the meter across the open switches on the card extender for pins C/A 16 for OUTPUT #1 and C/A 22 for OUTPUT #2.
6. Current readings should be 16 to 30 mAdc for a 2200 ohm resistor and 160 to 230 mAdc for a 25 ohm resistor.
7. Disconnect the Signal Generator from the jack (J1) on the rear panel.
8. Re-install the Keying Module.

Table 5–5. Receiver Output.

Terminal	Resistor Value (ohms/watt)	Battery Voltage (Vdc)	JU1/JU2 Position	Current limit (mA)
TB1-3	2200/2	48	48	20
TB1-8	2200/2	125	125/250	20
TB1-8	2200/2	250	125/250	20
TB1-3	25/5	48	48	200
TB1-3	25/5	125	125/250	200
TB1-8	25/5	250	125/250	200
TB1-6	2200/2	48	48	20
TB1-9	2200/2	125	125/250	20
TB1-9	2200/2	250	125/250	20
TB1-6	25/5	48	48	200
TB1-6	25/5	125	125/250	200
TB1-9	25/5	250	125/250	200

5.3.6 Optional Checkback System Tests

The jumper settings for the master checkback per Section 5.2.9 will generate a sequence of signals from the Master every hour. You may press the "manual initiate" (INITIATE) pushbutton (S3) on the front panel of the Master to initiate a sequence of events.

Master Checkback Test (without remote TC–10B)

1. Make sure the TC–10B transmitter (J1) is terminated with a 50 ohm load.
2. Initiate a checkback cycle by pushing switch S3 (the INITIATE pushbutton). The Master should send the following signals LL1, LLI, HLI, HL1, LL2, LL2, HL2, HL2, LL3, LL3, HL3, and HL3. All the test LEDs (LL1, HL1, LL2, HL2, LL3, HL3) should remain "ON" for approximately five (5) seconds. The LL DATA and HL DATA LED should blink twice for each test (LL1, HL1, etc.). The events should count six (6) errors for each manually initiated (by switch S3) cycle.

   With the jumpers set as in Section 5.2.9, the Master will scan all tests each time an initiate pulse is originated.
3. Move JU10 on the Master checkback to the A position. This will increase the speed of the checkback interval timer from one hour to 56.25 seconds. Every 56.25 seconds the Master should generate an initiate pulse and the Master should send each test twice (JU9-B).

Master and Remote Checkback Test

If two TC–10Bs are available, you can perform a back to back test to check both checkback units.

1. Connect both TC–10Bs for 2-wire operation and use a 20–40 dB attenuator between J1 on each TC–10B.
2. Adjust the Receiver for a 15 dB margin.
3. Set the jumpers on the Master checkback to send LL1 and HL1 to Remote 1.

MASTER	JU1 – A	(LL1)
	JU2 – B	(HL1)
	JU3 – C	(STOP)
	JU4 – D	
	JU5 – E	
	JU6 – F	

	A0	A1	A2	A3	A4
S5 TRANSMIT	DN	UP	DN	UP	DN
S6 RECEIVE	DN	UP	DN	UP	DN

The remote jumpers are already set except for the transmit and receive address:

	A0	A1	A2	A3	A4
S3 RECEIVE	DN	UP	DN	UP	DN
S2 TRANSMIT	DN	UP	DN	UP	DN

When you press the INITIATE pushbutton (S3), the Master should send LL1 and HL1 to the Remote, and the Remote should answer and turn off both LL1 and HL1 "TESTS" LEDs. The LL DATA and HL DATA LEDs should blink only once for each initiate pulse. The counter should not count any errors.

Remote Checkback Test

Press the INITIATE pushbutton (S1) on the Remote. The HL DATA LED should blink, followed by the LL DATA and the HL DATA LED. When the Remote is initiated, it commands the Master to send LL1 and HL1 to the Remote.

> NOTE
>
> This concludes the acceptance test for the Master and Remote Checkback. (For checkback Troubleshooting and Diagnostic testing refer to Chapter 18). Be sure to set jumper JU10 to B (normal) and S2 (Checkback Interval) to the proper binary number for the hours desired.

If the TC–10B Receiver is a G02 (Narrowband for TC–10B) and is operated in the 2-wire mode, it may be necessary to reduce the clock speed of the master and remote checkback, because the receiver cannot recover in time to receive the response from the remote checkback. If the narrow band receiver is operated in the 4-wire mode, then receiver saturation does not occur and normal checkback speed can be used.

5.3.7 Optional Voice Adapter Module Tests

Plug the handset into the (TJ1) front panel; if you have a remote handset, plug it into the remote panel connected to the rear panel (TB5). Key the carrier set with the push-to-talk switch on the handset. The Transmitter should be keyed at voice-level (4.3 W when high-level is 10 W).

> NOTE
>
> The alarm/alarm cutoff LED will be illuminated whenever the handset is plugged in.

The front control panel adjustments: "MIC. SENS" (R63) and "RECEIVE AUDIO" (R24) are factory set to nominal levels. You may turn the "MIC. SENS" adjustment clockwise to compensate for a low-efficiency microphone. You may turn the "RECEIVE AUDIO" adjustment as required to obtain a desirable listening level.

5.3.8 Final Frequency Settings

The following frequency adjustments are to be made after the TC–10B has completed a full one (1) hour warm-up period, and the modules have reached a stable operating temperature.

Transmitter (1610C01)

1. Remove the Transmitter Module from the chassis, and place it on an extender board (see Figure 4-1).
2. Set the four Transmitter dials to 250 kHz or any desired frequency.
3. Connect the 50 ohm resistor load to the UHF RF output jack (J1) on the Motherboard.
4. Connect the Frequency counter across the 50 ohm load.
5. Key the Transmitter to HL (10W).
6. Monitor between TP1 and common (A/C-30, 32) with the frequency counter. Adjust C19 for a frequency of 3.276800 MHz ±1.0 Hz.
7. Insert the Transmitter into the chassis. Recheck the Transmitter output as in Step 6.

Receiver

1. Remove the Receiver Module from the chassis and place it on an extender board (see Figure 4-1).
2. Connect the Frequency Counter (H/P 5381A) to the Receiver at TP1 (refer to sheet 2 of the Receiver schematic in Figure 14-4). Set the counter to measure 5 MHz. Adjust the crystal oscillator (C68) for 5 MHz + 2 Hz. Remove the counter from the junction.
3. Re-install the Receiver into the chassis.

Chapter 6. Routine Adjustment Procedures

You perform routine adjustments in the field for the following purposes:

- Verifying initial TC–10B factory adjustments.
- Adapting the TC–10B to your application.
- Setting the TC–10B operating frequencies.
- Periodic maintenance.

Be sure to run the adjustment tests in the following order:

1. Select the TC–10B Operating Frequency.
2. Review the Adjustment Data Sheets (at the end of this chapter); you should complete the data sheets as you perform the Adjustment Steps.
3. Select the TC–10B Keying Conditions.
4. Select the TC–10B Receiver Output.
5. Select the TC–10B Transmitter RF Output Impedance.
6. Check the Line Tuning and Matching Equipment.
7. Check the TC–10B Transmitter Power Levels.
8. Offset the TC–10B Transmitter Frequency.
9. Check the TC–10B Receiver Margin Setting and Remote Carrier Level Indicator.
10. Select the optional Checkback Module conditions.

To prepare the TC–10B for the routine adjustment tests, perform the following:

- Review the Test Equipment (Chapter 4).
- Review the Adjustment Data Sheets (at the end of this chapter); you should complete the data sheets as you perform the Adjustment Steps.
- Review the TC–10B Block Diagram as described under Signal Path (Chapter 7).
- Remove the cover from the front of the chassis. After removing the cover, set it in a safe place.

⚠ CAUTION

MAKE SURE THAT THE POWER HAS BEEN TURNED "OFF" USING THE POWER SWITCH (S1) ON THE POWER SUPPLY MODULE; THE INPUT (D3) AND OUTPUT (D11) LEDS SHOULD NOT SHOW RED LIGHTS.

If you are using the optional Alarm Relay, set jumper JU1 on the Power Supply Module.

6.1 Select the TC–10B Operating Frequency

1. Remove the Transmitter Module from the TC–10B chassis and select the operating frequency.
   a) Using the module extractors, remove the Transmitter Module.
   b) Select the Transmitter operating frequency (between 30 and 535 kHz), by turning the four Transmitter rotary programming switches (in 0.1 kHz steps), with a small screwdriver until the desired operating frequency appears through the (four) windows in the Transmitter control panel.
   c) Fold the module extractors flat against the front panel and insert the module back into the TC–10B chassis, by seating it with firm pressure.
2. Remove the Receiver Module from the TC–10B chassis and select the operating frequency.
   a) Using the module extractors, remove the Receiver Module.
   b) Select the Receiver operating frequency (between 30 and 535 kHz), by turning the four Receiver rotary programming switches (in 0.5 kHz steps), with a small screwdriver until the desired operating frequency appears through the (four) windows in the Receiver control panel.
   c) If the Receiver Module is to be disabled while the Transmitter Module is keyed, set jumper JU1 in the "DISABLE" position on the Receiver printed circuit board (PCB).
   d) Fold the module extractors flat against the front panel and insert the module back into the TC–10B chassis, by seating it with firm pressure.

6.2 Select TC–10B Keying Conditions

6.2.1 Keying Mechanisms

Keying mechanisms for the TC–10B are of two types:

- Control Panel source (e.g., using test push-buttons)
- Printed Circuit Board (PCB) source (e.g., using jumpers)

6.2.2 Keying Module Jumpers

1. Remove the Keying Module from the chassis and set jumpers JU1 through JU8 as desired (refer to Figures 2-5 through 2-16):

   JU1 – Keying Voltage Carrier Start
   - 15 V
   - 48 V
   - 125 V
   - 250 V

   JU2 – Keying Voltage Carrier Stop
   - 15 V
   - 48 V
   - 125 V
   - 250 V

   JU3 – Keying Voltage Low-Level Key
   - 18 V
   - 48 V
   - 125 V
   - 250 V

JU4 – Sense of Input Low-Level

- NORM (+)
- INVERT(-)

JU5 – Sense of Input Carrier Stop

- NORM (+)
- INVERT(-)

JU6 – Sense of Input Carrier Start

- NORM (+)
- INVERT (-)

JU7 – Priority Start or Stop

- STOP
- START

> **NOTE**
>
> You may use the "INVERT' positions on JU4 (LOW-LEVEL KEYING) and JU6 (HIGH-LEVEL KEYING) when it is impractical to hold down the (RECESSED) pushbuttons ("HL" and "LL") on the Keying Module control panel.

JU8 – Carrier Stop Circuit

OUT	Normally in this position
IN	When used with KDAR or SKBU applications

2. Two pushbutton switches are provided for test purposes:
   - The top pushbutton is marked "HL" for High-Level power (10 W typical)
   - The bottom pushbutton is marked "LL" for Low-Level power (1 W typical)

   Each pushbutton is recessed, and can be activated by sliding an object (e.g., a pen or pencil) through each pushbutton access location on the Keying Module front panel.
3. Check the LEDs at the bottom of the Keying Module control panel for indication of the keying condition: "HL" (High-Level key output), "LL" (Low-Level key output), and "V" (Voice-Level key output).

   The JU7 STOP position inhibits the High-Level output, Low-Level output, and the Voice-Level output.

   Both the Low-Level and High-Level outputs inhibit the Voice-Level output.
4. Insert the Keying Module back into the TC–10B chassis.

6.3 Select TC–10B Receiver Output

1. Remove the Receiver Output Module from the TC–10B chassis and set jumpers JU1 and JU2 according to the following options:

   JU1
   1) 48 V
   2) 125/250 V

   JU2
   1) 48 V
   2) 125/250 V
2. Insert the Receiver Output Module back into the TC–10B chassis.

6.4 Select TC–10B RF Output Impedance

1. Configure the RF Interface 2-Wire impedance. Remove the RF Interface Module from the TC–10B chassis and configure the output impedance by setting the jumpers as follows:
   - JU4, when set, provides 50 ohms
   - JU3, when set, provides 75 ohms
   - JU2, when set, provides 100 ohms
2. Select 2- or 4-wire Receiver input, using jumpers JU1 and JU5 as follows: IN position for 2-wire; OUT position for 4-wire.
3. Set jumper JU6 to the desired Receiver sensitivity range.
4. Insert the RF Interface Module back into the TC–10B chassis.

6.5 Check Line Tuning And Matching Equipment

1. Refer to the appropriate instructions for line tuning equipment.
2. Perform the required adjustments.

⚠ CAUTION

DO NOT ALLOW INEXPERIENCED PERSONNEL TO MAKE THESE ADJUSTMENTS. PERSONNEL MAKING THE ADJUSTMENTS MUST BE COMPLETELY FAMILIAR WITH THE HAZARDS INVOLVED.

6.6 Check TC–10B Transmitter Power Levels

With power "OFF", remove the coaxial cable connection to the Hybrids or line tuning equipment and substitute a 50, 75 or 100 ohm resistor termination (in accordance with the jumper settings in 6.3-1).

Check High-Level Output

1. Connect the Selective Level Meter to the 10W PA Module control panel at the test jacks:

   TJ1 Input (top jack)

   TJ2 Common (bottom jack)
2. Tune the meter to the Transmitter frequency.
3. Turn power "ON" at the Power Supply Module.

NOTE

The INPUT and OUTPUT LEDs should show red.

4. On the Keying Module control panel, press and hold the top pushbutton (marked "HL"), to key the Transmitter at High Level power.

NOTE

The "HL" LED should show red.

5. Record the Selective Level Meter reading (at TJ1, TJ2). The meter should measure .224 Vrms (0 dBm at 50 ohm reference) for full High-Level keying (10 W power). If the meter measures 0 dBm, skip to Step 8.
6. If the meter does not measure 0 dBm, turn power "OFF" at the Power Supply Module and remove the Transmitter Module from the chassis. Place the extender board into the Transmitter Module position of the chassis. Then plug the Transmitter Module onto the extender board.
7. Adjust the 10 W potentiometer (R13) on the Transmitter Module until the Selective Level Meter (at the 10W PA TJ1, TJ2) reads .224 Vrms (0 dBm at 50 ohm reference). Then place the Transmitter Module back in the chassis.
8. On the Keying Module control panel, release the "HL" pushbutton to un-key the Transmitter Module.

NOTE

The "HL" LED should not be red.

Check Low-Level Output

With the conditions the same as for the High-Level output check, i.e.,

- Selective Level Meter at 10W PA Module control panel (TJ1, TJ2)
- Meter tuned to XMTR frequency
- Power "ON"

do the following:

1. On the Keying Module control panel, press the bottom pushbutton (marked "LL"), to key the Transmitter at Low Level power.
2. Record the Selective Level Meter reading (at TJ1, TJ2). The meter should measure .0707 Vrms (-10 dBm at 50 ohm reference) for Low-Level keying (1 W power). If the meter measures -10 dBm, skip to Step 6.

3. If the meter does not measure -10 dBm, turn power "OFF" at the Power Supply Module, and remove the Transmitter Module from the chassis. Place the extender board into the Transmitter Module position of the chassis. Then plug the Transmitter Module onto the extender board.
4. Adjust the 1 W potentiometer (R12) on the Transmitter Module, until the Selective Level Meter (at the 10W PA TJ1, TJ2) reads 0707 Vrms (-10 dBm at 50 ohm reference). Then place the Transmitter Module back in the chassis.

> NOTE
>
> We recommended that you set the low level power 10 dB below full power. However, you may use any power level between 10 W and 50 mW.

5. On the Keying Module control panel, release the "LL" pushbutton to un-key the Transmitter Module.

> NOTE
>
> The "LL" LED should not be red.

Check Voice-Level Output

Perform this procedure only if you are using the Voice Level Option.

With the conditions the same as for the High-Level output check, i.e.,

- Selective Level Meter at 10W PA Module control panel (TJ1, TJ2)
- Meter tuned to XMTR frequency
- Power "ON"

do the following:

1. Key the carrier set with the Push-to-Talk switch (on the handset), while muting the microphone, to key the Transmitter at Voice-Level (4.3 W power, when High-Level is 10 W power).

> NOTE
>
> The "V" LED should show red.

2. Record the Selective Level Meter reading (at TJ1, TJ2). The meter should measure .148 Vrms (-3.6 dBm at 50 ohm reference) for Voice Keying. If the meter measures -3.6 dBm, skip to Step 5.
3. If the meter does not measure -3.6 dBm, turn power "OFF" at the Power Supply Module and remove the Transmitter Module from the chassis. Place the extender board into the Transmitter Module position of the chassis.

> NOTE
>
> If a full power level (other than 10 W) is used, the VF level should be set accordingly, i.e., 3.6 dB below the High-Level value.

Then plug the Transmitter Module onto the extender board.

4. Turn the Voice Adjust potentiometer (R14), on the Transmitter Module, until the Selective Level Meter (TJ1, TJ2) reads .148 Vrms (-3.6 dBm at 50 ohm reference). Then place the Transmitter back in the chassis.
5. Monitor the output of the carrier set with an oscilloscope at the 10W PA Module test jacks:
   - TJ1
   - TJ2
6. Voice key the Transmitter by pushing the Push-to-Talk switch (on handset) and using the signal generator at 1 kHz (TB5/2 and 3) to set the level to achieve the following voltages:
   - ∪ 62 Vp-p (at peak modulation)
   - ∪ 20 Vp-p (valley)
7. If the ratio of the voltages (0.62/0.20) do not approximate a value of 3, adjust potentiometer R11 on the Transmitter, as follows:

- Clockwise if not enough signal (a value less than 3).
- Counterclockwise if too much signal (a value significantly greater than 3).

8. Un-key the Push-to-Talk switch (on handset).

Adjust the Transmitter Power Output Levels

1. Move the Selective Level Meter to the test jacks marked "LINE" (on the RF Interface control panel): TJ1 (Line – top jack) and TJ2 (Common – bottom jack)

> NOTE
>
> The "LL" LED should show red.

2. On the Keying Module control panel, press and hold the bottom ("LL") pushbutton to key the Transmitter at Low-Level power.
3. On the RF Interface Module control panel, configure the output impedance by setting a Jumper. The Selective Level Meter (TJ1, TJ2) should show a maximum reading (Vrms) for 1 W (+30 dBm) power, as follows:
   - JU4, when set, provides 50 ohms (7.07 Vrms)
   - JU3, when set, provides 75 ohms (8.6 Vrms)
   - JU2, when set, provides 100 ohms (10.0 Vrms)
4. If the above (Vrms) values are not achieved, adjust the "INPUT LEVEL SET" potentiometer (R53) on the 10W PA Module control panel to obtain 7.07 Vrms (for 50 ohms reference).
5. On the Keying Module control panel, release the "LL" pushbutton to unkey the Transmitter Module.
6. Check the High-Level key for 10 W output.
7. Turn power "OFF" at the Power Supply Module.

> NOTE
>
> If you want a final output power of less than 10 W, reduce power by adjusting the input level potentiometer (R53) on the 10W PA Module for the lower power. If a sufficiently low level is not obtainable using R53, repeat the above alignment procedures using the reduced level.

8. Remove the 50, 75, or 100 ohm resistor termination and replace the coaxial cable connection to the Line Tuner.

6.7 Offset TC–10B Transmitter

> NOTE
>
> Customer personnel should use voice communications while working simultaneously, with transmitter #1 (near end) and transmitter #2 (far end), to perform the following procedure:

Frequency

It the Transmitter frequency needs to be offset (for- three-terminal line applications), monitor the Transmitter frequency with a Frequency Counter.

1. Make sure that the power is "OFF" at the Power Supply Module and remove the Transmitter Module from the chassis. Place the extender board into the chassis in the Transmitter Module position. Then plug the Transmitter Module onto the extender board.
2. On the RF Interface Module, connect the Frequency Counter to test jacks marked Line In (TJ1) and Common (TJ2)
3. At the Power Supply Module, turn "ON" power.
4. On the Keying Module, push either the "HL" or "LL" test buttons.
5. On the Transmitter Module, turn rotary switch S4 to raise or lower the Transmitter frequency (in 100 Hz steps) as follows:

a) At Transmitter #1 (near end), turn rotary switch S4 clockwise to raise the frequency (should be set at +100 Hz offset).

NOTE

The third terminal's transmitter should remain at center frequency.

b) At Transmitter #2 (far end), turn rotary switch S4 counterclockwise to lower the frequency (should be set at -100 Hz offset).

NOTES:

1. **The foregoing procedure adjusts the Receiver margin to the recommended 15 dB value.**
2. **If the TC–10B is equipped with an internal CLI meter, the meter reading should be 0 dB at this time.**
3. **In three-terminal line applications, the margin adjustment procedure should use the weaker of the two received signals.**
4. **When applying the TC–10B with a SKBU relay, do not readjust the Receiver level when keying with a square wave signal. The CLI will read around -10 dB, but this is an average reading of the on and off square wave. The receiver will still maintain the 15 dB margin. The CLI reading is only accurate for a non-amplitude modulated signal (CW).**

6. At the Power Supply Module, turn power "OFF".
7. Remove the Transmitter Module from the extender board and replace it in the TC–10B chassis.
8. Recheck the Transmitter frequency (with the Transmitter in the chassis), using Steps 2 through 5 above.

NOTE

If you are using an external CLI meter without the internal one, do not perform Step 2 (below); go directly to Step 4.

6.8 Check TC–10B Receiver Margin Setting And Remote Signal Level Indicator

NOTE

On a 3-terminal line, use the remote that results in the lowest received signal level.

1. At the Power Supply Module, turn the power "ON".
2. On the Keying Module of the Remote Transmitter, push the "HL" test button to provide a normal received signal.

3. On the Receiver Module (local receiver) control panel, turn the "INPUT LEVEL ADJ" potentiometer (R3) for greater or less Receiver margin sensitivity. Turn R3 counter-clockwise until the "MARGIN" LED on the Level Detector Module goes out. Then turn R3 clockwise until the "MARGIN" LED just lights.
4. If you are using an external CLI meter:
   a) At the Power Supply Module, turn power "OFF".
   b) Remove the Level Detector Module from the chassis. Place the extender board into the chassis in the Level Detector position. Then plug the Level Detector Module onto the extender board.
   c) At the Power Supply Module, turn power "ON".
   d) Press the "HL" (High-Level) pushbutton on the Keying Module of the remote transmitter.
   e) On the Level Detector Module, turn potentiometer R61 (labeled "EXTERNAL CLI"), so that the external CLI meter reads +10 dB.
5. On the Level Detector Module:
   a) Adjust potentiometer R18 for the desired threshold switch level.
   b) Adjust potentiometer R23 for the desired margin switch level.
   c) Set jumper JU1 for margin relay alternate contact states.
6. At the Power Supply Module, turn power "OFF".
7. Remove the Level Detector Module from the extender board and place the Level Detector Module in the chassis.

> NOTE
>
> When placing the TC–10B into service, refer to the "instruction leaflet' that is appropriate for the relay system you are using with the TC–10B system.

6.9 Select Optional Checkback Module Conditions

If you are using the optional Automatic Checkback system, select the desired conditions for the Automatic Checkback Module's operation.

6.10 Prepare TC–10B for Operation

1. Be sure that power is “ON” at the Power Supply Module.
2. Replace the cover on the TC–10B control panel. Secure both latches by pushing inward and sideways until the cover is secure. You may lock the latches in place using meter seals.

This completes the “Routine Alignment” procedure. The TC–10B is ready to be put into operation.

TC–10B ADJUSTMENT DATA SHEET

(1) Power Supply

+20 V . . . . . .(TJ1/TJ2) _____

-20 V . . . . . .(TJ3/TJ2) _____

LEDS “ON” . . . . . — _____

(2) 10W PA

Voice PA “IN” . . . . . .(TJ1/TJ2) _____

LLPA “IN” . . . . . .(TJ1/TJ2) _____

HLPA “IN” . . . . . .(TJ1/TJ2) _____

LEDS “ON” . . . . . — _____

(3) RF Interface

Residual Noise “OUT” . . . . . .(TJ1/TJ2) _____

XMTR Frequency “OUT”, ...(TJ1/TJ2) _____

Voice Line “OUT” . . . . . .(TJ1/TJ2) _____

LL Line “OUT” . . . . . .(TJ1/TJ2) _____

HL Line “OUT” . . . . . .(TJ1/TJ2) _____

Residual Noise “OUT” w/XMTR Keyed . . . . . .(TJ1/TJ2) _____

Received Frequency, ...(TJ3/TJ4) _____

Received Line Level . . . . . .(TJ3/TJ4) _____

(4) Receiver

Input Level . . . . . .(TJ1/TJ3) _____

Received Level . . . . . .(TJ2/TJ3) _____

_____ _____

(5) CLI (From Other End)

LL Keyed . . . . . .(dB) _____

HL Keyed . . . . . .(dB) _____

Margin LED . . . . . – _____

Detect LED . . . . . – _____

(6) Receiver Output

Output 1 . . . . . .(48 V) _____

Output 1 . . . . . .(125/250 V) _____

Output 2 . . . . . .(48 V) _____

Output 2 . . . . . .(125/250 V) _____

(7) Rear of Chassis

Reflected Power . . . . . .(J1) _____ (%)

Test Performed By **Date**

TC–10B JUMPER SETTINGS

(1) POWER SUPPLY

JU1	Power Alarm	NO _	NC _

(2) KEYING

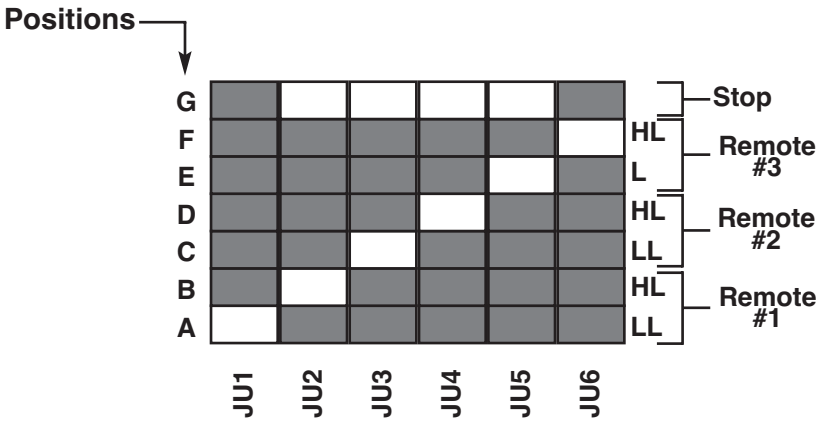
JU1	Carrier Start	15 V _	48 V _	125 V _	250 V _
JU2	Carrier Stop	15 V _	48 V _	125 V _	250 V _
JU3	Low Level Key	15 V _	48 V r	125 V _	250 V _
JU4	Low Level	INV _	NORM _		
JU5	Stop	INV _	NORM _		
JU6	Start	INV _	NORM _		
JU7	Stop/Start Priority	Stop _	Start _		
JU8	KA-4/SKBU-1 (Common Start/Stop Lead? Yes = IN; No = OUT)	IN _	OUT _		

(3) 10W POWER AMPLIFIER

JU1	Power Monitor	NO _	NC _

(4) RF INTERFACE

JU1	2 Wire/4 Wire	IN _ (2 Wire)	OUT _ (4 Wire)



NOTE: The white blocks indicate the most commonly used jumper positions.

JU2	Impedance – 100 Ω	IN _	OUT _
JU3	Impedance – 75 Ω	IN _	OUT _
JU4	Impedance – 50 Ω	IN _	OUT _
JU5	2 Wire/4 Wire	IN _ (2 Wire)	OUT _ (4 Wire)
JU6	Sensitivity	HIGH _	NORM _

(5) RECEIVER

JU1	Normal/Disable	NORMAL _	DISABLE _

(6) LEVEL DETECTOR and CLI

JU1	Margin Contact	NO _	NC _

(7) RECEIVER OUTPUT

JU1	Output #1	48 V _	125/250 V _
JU2	Output #2	48 V _	125/250 V _

(8) VOICE

JU1	Squelch	IN _	OUT _
JU2	Compressor	IN _	OUT _
JU3	Expandor	IN _	OUT _
JU4	Signaling	TC _	TCF _
JU5	Alarm Contact	NO _	NC _

(9) CHECKBACK MASTER

JU7	Clock Frequency	A _	B _	C _	D _	E _	F _
JU8	Response Interval	1 sec _	2 sec _	3 sec _	4 sec _		
JU9	Retry on Failure	A _	B _				
JU10	CB Interval Timer	A _	B _				
JU11	Stop After Failure	A _	B _				
JU12	Alarm	MOM _	SEAL IN _				
JU13	Events Counter	A _	B _	C _	D _	E _	F _ G _ H _ I _

JU14	Auto Initiate	A _ B _
JU15	Supv. Control Initiate	15 V _ 48 V _ 125 V _ 250 V _
S2	CB Interval	1 _ 2 _ 4 _ 8 _ 16 _ 32 _ 64 _ 128 _ **(Indicate "C" for CLOSE or "O" for OPEN)**
S5	Transmit System Address	A0 _ A1 _ A2 _ A3 _ A4 _
S6	Receive System Address	A0 _ A1 _ A2 _ A3 _ A4 _
S7*	Pulses/Hour (division factor)	1 _ 2 _ 3 _ 4 _ 5 _ 6 _ 7 _ 8 _
S8*	Pulses/Hour (division factor)	1 _ 2 _ 3 _ 4 _ 5 _ 6 _ 7 _ 8 _

*Fill in with "0" (Up) or "1" (Down)

(10) REMOTE

JU1	Remote Module	1 _ 2 _ 3 _
JU2	Daisy Chain or Normal	A _ Daisy B _ Normal
JU3	Supv. Control Initiate	15 V _ 48 V _ 125 V _ 250 V _
JU4	Daisy Chain	15 V _ 48 V _ 125 V _ 250 V _
JU5	Clock Frequency	A _ B _ C _ D _ E _ F _
S2	Transmit System Address	A4 _ A3 _ A2 _ A1 _ A0 _
S3	Receive System Address	A4 _ A3 _ A2 _ A1 _ A0 _

Chapter 7. Signal Path

The following description of the TC–10B signal path is in accordance with the Functional Block Diagram (see Figure 7-1) and the Rear Panel previously shown (in Figure 3-1). You may find this discussion of signal path useful during Acceptance Testing (Chapter 5) and Routine Adjustment (Chapter 6).

7.1 Power Supply Module

Terminal Block (TB7)

TB7-1 Positive Vdc (also pins C/A-12 and C/A-10)

TB7-2 Negative Vdc (also pins C/A-14)

TB7-3 Failure Alarm Signal (also pins C/A-16)

> NOTE
>
> The Vdc is received from three (3) available groups of station batteries:
>
> - 38–70 Vdc (48–60 Vdc nominal)
> - 88–140 Vdc (110–125 Vdc nominal)
> - 176–280 Vdc (220–250 Vdc nominal)

TB7-4 Failure Alarm Signal (also pins C/A-18)

TB7-5 Spare Chassis Ground

TB7-6 Chassis Ground

Voltage Output to All Other Modules

Positive voltage outputs (+20 Vdc) are available at pins A-2 and A-4, while negative voltage outputs (-20 Vdc) are available at pins C-2 and C-4. Common to ground (pins C/A-30 and C/A-32).

Optional low-voltage power alarm relay outputs

Optional low-voltage power alarm relay outputs are available at pins C/A-16 and C/A-18.

7.2 Keying Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Terminal Block (TB4)

TB4-1 Carrier (CXR) Start + (also pin A-10).

TB4-2 Carrier (CXR) Start - (also pin C-10).

TB4-3 CXR Stop + (also pin C-16).

TB4-4 CXR Stop - (also pin A-16).

TB4-5 Low-Level Key + (also pin A-22).

TB4-6 Low-Level Key - (also pin C-22).

Optional Inputs:

Checkback Test, High-Level Key	Pin C-8
Checkback Test, Low-Level Key	Pin C-28
Voice Key	Pin C-24

Outputs to Transmitter Module

High-Level (10-W) Key	Pin A-8
Voice (4.3-W) Key	Pin A-6
Any Transmitter Key	Pin C-6

Output to Receiver Module

Any Transmitter Key	Pin C-6

7.3 Transmitter Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Inputs from Keying Module (4 V Standby, 19 V Keyed)

High-Level (10-W) Key	Pins C/A-8
Voice (4.3-W) Key	Pins C/A-6
Any Transmitter Key	Pin A-10

Input from Optional Voice Adapter Module:

AM Voice	Pins C/A-26

Output to 10W PA Module

0 dBm for 10 W or -10 dBm for 1 W Transmitter output power	Pins C/A-28

7.4 10W PA MODULE

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Terminal Block (TB3)

TB3-1	Optional RF Output Alarm (pins C/A-12)
TB3-2	Optional RF Output Alarm (pins C/A-14)

Input from Transmitter Module

0 dBm for 10 W output or -10 dBm for 1 W output	Pins C/A-28

Output to RF Interface Module

1 W, 4.3 W or 10 W PA RF output	Pins C/A-16 and C/A-18

7.5 RF Interface Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Input from 10W PA Module

1 W, 4.3 W or 10 W PA output power	Pins C/A-16 and C/A-18

Output to Receiver Module

RF Output Signal	Pins C/A-28

Other Outputs

1) Cable Jacks

   J1 RF Interface module (C/A-12 and C/A-10) Transmitter RF output line, through coaxial cable (UHF)

   J2 RF Interface module (C/A-24 and C/A-22) Receiver RF input line through 5,000 ohm coaxial cable (BNC)

2) Jumpers

JU1, JU5	2-wire or 4-wire
JU2, JU3, JU4	50, 75, or 100 ohm output impedance

7.6 Receiver Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Input from Keying Module

Any Transmitter Key	Pin C-6

Input from RF Interface Module

RF Input Signal	Pin C-28

Output to Detector CLI Module

20 kHz signal	Pin A-28

RF Output to Optional Voice Adapter

20 kHz signal	Pin A-28
5.02 mHz signal	Pins C/A-24

7.7 Level Detector And CLI Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Input from Receiver Module

20 kHz signal	Pins C/A-24

Terminal Block (TB2)

TB2-1 Optional External CLI Meter (pins C/A-12)

TB2-2 Optional External CLI Meter (pins C/A-14)

TB2-3 Detect Level Indication (pins C/A-16)

TB2-4 Detect Level Indication (pins C/A-18)

TB2-5 Margin Level Indication (pins C/A-20)

TB2-6 Margin Level Indication (pins C/A-22)

Output to Receiver Output Module

Positive (+l0 Vdc) output voltage	Pin C-28
Negative return for +10 Vdc	Pin A-28

Output to Optional Checkback Module

Positive output voltage (+20 Vdc) whenever the 20 kHz signal exceeds the DETECT level of 0.177 Vp-p (pins C/A-6)

7.8 Receiver Output Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Input from Level Detector Module

Positive (+10 Vdc) Output Voltage	Pins C/A-26
Negative return for +10 Vdc	Pins C/A-28

Terminal Block (TB1)

TB1-1 “In 1+”	Positive side of external source voltage 40– 300 Vdc
TB1-2 “1A Out 1”	1 Amp output
TB1-3 “Out 1”	Output for 200 mA (48 or 125 Vdc) or 20 mA (48 Vdc)
TB1-4 “In 2+”	(Same use as TB1-1)
TB1-5 “1A Out 2”	(Same use as TB1-2)
TB1-6 “Out 2”	(Same use as TB1-3)
TB1-7	(Unused at this time)
TB1-8 “Out 1C”	Output for 20 mA (125 or 250 Vdc) or 200 mA (250 Vdc)
TB1-9 “Out 2C”	(Same as TB1-8)

7.9 Optional Checkback Modules

Two different modules are represented:

- Master
- Remote

7.9.1 Connections that are Identical for Both Master and Remote Modules

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

Input from Level Detector Module

Positive input voltage (+20 Vdc) whenever the 20 kHz signal exceeds the DETECT level of 0.177 VP-P (pin C-6)

Terminal Block (TB6-1, 2, and 3)

TB6-1	Positive (+) Supervisory Control Initiate (pins C/A-8)
TB6-2	Negative (-) Supervisory Control Initiate (pins C/A-10)
TB6-3	Unused (pins C/A-12)

Outputs to Keying Module

High-Level Key	Pin A-6
Low-Level Key	Pin A-28

7.9.2 Connections that are Different for Master and Remote Modules

Master Module Inputs

Optional Events Counter Relay, Normally Closed	TB5-7 and pin A-22
Optional Events Counter Relay, Common	TB5-8 and pin A-24
Optional Events Counter Relay, Normally Open	TB5-9 and pin A-26

Master Module Outputs

High-Level Failure, Normally Closed	TB6-4 and pins C/A-14
High-Level Failure, Common	TB6-5 and pins C/A-16
High-Level Failure, Normally Open	TB6-6 and pins C/A-18
Low-Level Failure, Normally Closed	TB6-7 and pin C-22
Low-Level Failure, Common	TB6-8 and pin C-24
Low-Level Failure, Normally Open	TB6-9 and pin C-26

Remote Module Inputs

Daisy Chain High-Level Receive-In	TB5-7 and pin A-22
Daisy Chain Low-Level Receive-In	TB5-8 and pin A-24
Daisy Chain Receive Common	TB5-9 and pin A-26

Remote Module Outputs

TB6-4	Not used
TB6-5	Not used
TB6-6	Not used
Daisy Chain High-Level Send-Out	TB6-7 and pin C-22
Daisy Chain Low-Level Send-Out	TB6-8 and pin C-24
Daisy Chain Send Common	TB6-9 and pin C-26

7.10 Optional Voice Adapter Module

Voltage Inputs

+20 Vdc	Pins A-2 and A-4
-20 Vdc	Pins C-2 and C-4
Common	Pins C/A-30 and C/A-32

RF Input from Receiver Module

- 20 kHz signal through jumper JU4
- 5.02 mHz signal through jumper JU3 (both signals at pins C/A-26) (JU3 and JU4 on backplane)

Output to Keying Module Voice Key

Pins C/A-22

Output to Transmitter Module AM Voice

Pin A-28

TABLE A. CHECKBACK SIGNAL NAMES AND CONNECTIONS		
	REMOTE CHECKBACK	MASTER CHECKBACK
TB5 PIN 7	DAISY CHAIN H.L. RECEIVE IN	EVENTS NORMALLY CLOSED
TB5 PIN 8	DAISY CHAIN L.L. RECEIVE IN	EVENTS COMMON
TB5 PIN 9	DAISY CHAIN RECEIVE COMMON	EVENTS NORMALLY OPEN
TB6 PIN 3	NOT USED	NOT USED
TB6 PIN 4	NOT USED	HIGH LEVEL FAILURE NORMALLY CLOSED
TB6 PIN 5	NOT USED	HIGH LEVEL FAILURE COMMON
TB6 PIN 6	NOT USED	HIGH LEVEL FAILURE NORMALLY OPEN
TB6 PIN 7	DAISY CHAIN H.L. SEND OUT	LOW LEVEL FAILURE NORMALLY CLOSED
TB6 PIN 8	DAISY CHAIN L.L. SEND OUT	LOW LEVEL FAILURE COMMON
TB6 PIN 9	DAISY CHAIN SEND COMMON	LOW LEVEL FAILURE NORMALLY OPEN

* = NOT USED ON TC–10B

** = VOLTAGE INDICATED AS STAND BY/KEYED

△ – 3500 OHM, 5 W FOR 125 Vdc (20 mA) OUTPUT

– 500 OHM, 40 W FOR 250 Vdc (200 mA) OUTPUT

– 9200 OHM, 10 W IN SERIES WITH 500 OHM, 40 W FOR 250 Vdc (20 mA) OUTPUT

– NOT USED FOR 125 Vdc (200 mA) OR 48 Vdc (20 OR 200 mA) OUTPUT

NOTE:

RF CONNECTORS J1 AND J2 AND TERMINAL BLOCKS TB1–TB7 ARE MOUNTED ON REAR OF CHASSIS. ALL CUSTOMER CONNECTIONS ARE MADE TO TB1–TB7 AND J1 AND J2.

FRONT PANEL TEST JACK · SWITCH · FRONT PANEL ADJUSTMENT · TELEPHONE TYPE JACK · SYNTHESIZER PROGRAMMING SWITCH

CLI METER · CHASSIS GROUND · LED INDICATOR · CURRENT SOURCE · JUMPER · RF CONN.

CAUTION: DO NOT CONNECT TB1-2 OR TB1-5 TO STATION NEGATIVE..

Figure 7–1. TC–10B Interconnection and Block Diagram. (1353D61)

Chapter 8. Maintenance

When individual module maintenance is required, either at the factory or at the customer installation (beyond the scope of routine alignment), the following procedures are applicable.

8.1 Precautions When Selecting Test Equipment

(See Chapter 4, Test Equipment for test equipment specifications.)

To prevent damage to solid-state components and circuits:

1) Use transformer-type signal generators, VTVMs and signal tracers, which isolate the test equipment from the power line. Whenever the test equipment uses a transformerless power supply, use an isolation type transformer. The test equipment ground should be isolated from the ac source ground.
2) Use multimeters with at least 20,000 Ohms-per-volt sensitivity.

⚠ CAUTION

HIGH CURRENTS FROM A LOW-SENSITIVITY METER CAN DAMAGE SOLID STATE DEVICES.

8.2 Precautions When Using Test Equipment

1. Use a common ground between the chassis of the test equipment and the transistor equipment.

⚠ CAUTION

METERING TRANSISTOR CIRCUITS CAN CAUSE DAMAGE. FOR EXAMPLE: A BASE-TO-COLLECTOR SHORT DURING TRANSISTOR OPERATION CAN DESTROY THE TRANSISTOR.

2. When testing transistors and diodes, give special attention to the polarity of the meter leads.

   For example: When measuring the forward resistance of a diode using a meter that has the internal battery connected to the metering circuit, be sure that:

   - The lead marked (+) touches the diode anode.
   - The lead marked (–) touches the diode cathode.

3. When checking circuits with an oscillographic probe, be sure to discharge any built-up capacitive voltage by touching the probe to a ground before touching the circuit.

8.3 Periodic Checks

Every six months, take the following readings on the TC–10B Test Jacks (at the control panel).

We recommend that you keep a ***log book*** as a visible record of periodic checks, as well as a source for indicating any gradual degradation in a module's performance.

8.3.1 Power Supply Module

TJ1 +20 Vdc

TJ2 Common

TJ3 -20 Vdc

8.3.2 Keying Module

None.

8.3.3 Transmitter Module

None.

8.3.4 10W PA Module

TJ1 Input

TJ2 Common

8.3.5 RF Interface Module

TJ1 Line In

TJ2 Line Common

TJ3 Receiver In

TJ4 Receiver Common

8.3.6 Receiver Module

TJ1 Input

TJ2 Receive

TJ3 Common

8.3.7 Level Detector and CLI Module

None.

8.3.8 Receiver Output Module

None.

8.3.9 Optional Automatic Checkback Modules

None.

8.3.10 Optional Voice Adapter Module

None.

8.4 Inspection

A program of routine visual inspection should include:

- Condition of cabinet or other housing
- Tightness of mounting hardware and fuses
- Proper seating of plug-in relays and sub-assemblies
- Condition of internal and external wiring (the location where external wiring enters the cabinet should be sealed)
- Appearance of printed circuit boards and components
- Signs of overheating in equipment:
  - Interference with proper heat dissipation from surfaces
  - Clogged air vents (air filters should be removed and washed out)
- Dust which may cause short-circuits

8.5 Solid-State Maintenance Techniques

Use the following techniques when servicing solid state equipment.

⚠ CAUTION

WE RECOMMEND THAT THE USER OF THIS EQUIPMENT BECOME ACQUAINTED WITH THE INFORMATION IN THESE INSTRUCTIONS BEFORE ENERGIZING THE TC–10B AND ASSOCIATED ASSEMBLIES. FAILURE TO OBSERVE THIS PRECAUTION MAY RESULT IN DAMAGE TO THE EQUIPMENT.

YOU SHOULD NEITHER REMOVE OR INSERT PRINTED CIRCUIT MODULES WHILE THE TC–10B IS ENERGIZED. FAILURE TO OBSERVE THIS PRECAUTION CAN RESULT IN COMPONENT DAMAGE.

ALL INTEGRATED CIRCUITS USED ON THE MODULES ARE SENSITIVE TO AND CAN BE DAMAGED BY THE DISCHARGE OF STATIC ELECTRICITY. BE SURE TO OBSERVE ELECTROSTATIC DISCHARGE PRECAUTIONS WHEN HANDLING MODULES OR INDIVIDUAL COMPONENTS.

8.5.1 Preliminary Precautions

1. To avoid damage to circuits and components from a current surge, disconnect power before replacing or removing components or circuits.
2. Before placing new components into a defective circuit, check the circuit so that it cannot damage the new components.

8.5.2 Trouble-Detection Sequence

1. Evaluate test jack readings and other records of routine alignment.
2. Evaluate any symptoms detected audibly or visually.
3. Replace suspected plug-in components.
4. Further isolation of faults includes:
   - Voltage readings
   - Resistance readings
   - Signal injection
   - Re-alignment
   - Sensitivity measurements
   - Gain measurements
5. Replace suspected faulty components.
6. Check-out and adjust affected circuits.

8.5.3 Servicing Components Soldered Directly to Terminals

1. Avoid overheating from soldering by using a low-wattage soldering iron (i.e., 60 watt maximum).
2. Make sure there is no current leakage from the soldering iron.

> NOTE
>
> You may use an isolation transformer to prevent current leakage.

3. When soldering leads from transistors or diodes, use heat sinks, e.g., alligator clips.
4. You can remove molten solder from the board with a solder-sucker.
5. When removing a multi-lead component from a printed circuit board, first cut all leads and then remove the leads individually (to prevent overheating). If there are only a few leads, you can use a broad-tip soldering iron.

8.5.4 Servicing Components Mounted Directly on Heat Sinks

1. Remove the heat sink and bracket from the chassis by loosening the securing devices.
2. Remove the transistor, diode, or other device from the heat sink.
3. When replacing the transistor, diode, or other device, make certain that the device and the heat sink make secure contact for good heat dissipation. Mount a device first on the heat sink, and then on the board. Also, make sure that you replace all insulators, washers, spring washers and other mounting hardware as you originally found them.

> NOTE
>
> We recommend a very light coating of DC-4 (Dow-Corning 4 Compound Silicon Lubricant) for transistors and diodes that are mounted on heat sinks.

8.5.5 Servicing Metal Oxide Semiconductor (MOS) Devices

MOS devices may be vulnerable to static changes. Be sure to observe the special precautions described below both before and during assembly.

> **⚠ CAUTION**
>
> **AVOID THE POSSIBILITY OF ELECTROSTATIC DISCHARGE.**

Precautions to take before assembly

- Avoid wearing silk or nylon clothing, as this contributes to static buildup.
- Avoid carpeted areas and dry environments.
- Discharge body static by placing both hands on a metal, earth-grounded surface.

Precautions to take during assembly

- Wear a ground strap during assembly
- Avoid touching electrically conductive circuit parts by hand
- When removing a module from the chassis, always place it on a conductive surface which is grounded through a resistance of approximately 100K Ohms
- Make sure that all electrically powered test equipment is properly grounded.

> NOTE
>
> Before touching a module with a test probe, connect the ground lead from the test equipment to the module. Always disconnect the test probe before removing the ground lead equipment.

Chapter 9. Power Supply Module

Schematic	1617C38-2
Parts List	1617C38-2

Table 9–1. 1617C38 Styles and Descriptions.

Group	Description
G01	48 V WITH ALARM RELAY
G02	125 V WITH ALARM RELAY
G03	250 V WITH ALARM RELAY
G04	48 V WITHOUT ALARM RELAY
G05	125 V WITHOUT ALARM RELAY
G06	250 V WITHOUT ALARM RELAY

9.1 Power Supply Module Description

The Power Supply Module for the TC–10B/TCF–10B has dual dc/dc high-frequency switching regulators which generate regulated voltage outputs of ±20 Vdc (between 1.5 and 2.0 Amps) for operation of the TC–10B/TCF–10B modules. It also provides protection from battery surge, transients, short circuits, and reverse voltage. The Power Supply Module can receive inputs from three available groups of station batteries: 38-70 Vdc, 88-140 Vdc, and 176-280 Vdc.

9.1.1 Power Supply Control Panel

(This panel is shown in Figure 1-1.)

Front panel controls are as follows:

1) Pushbutton Switch (with power-on indicator), ON/OFF (S1).
2) LEDs for indicating power:
   - INPUT, Red (LED1)
   - OUTPUT, Red (LED2)
3) Test Jacks:
   - +20 Vdc, Red (TP3)
   - Common, Green (TP2)
   - -20 Vdc, Black (TP1)

An optional low-voltage alarm relay indicating loss of power is available. When the alarm is activated, LED2 is “OFF”. LED1 may be “OFF” if input power is lost.

9.1.2 Power Supply PC Board

Figure 9-1 shows component locations for the Power Supply Module.

Control is as follows:

Jumper J1 for optional Alarm Relay; establishes loss of power condition (NO/NC).

NOTE

When the alarm is part of the system, JU1 is shipped in the NC state.

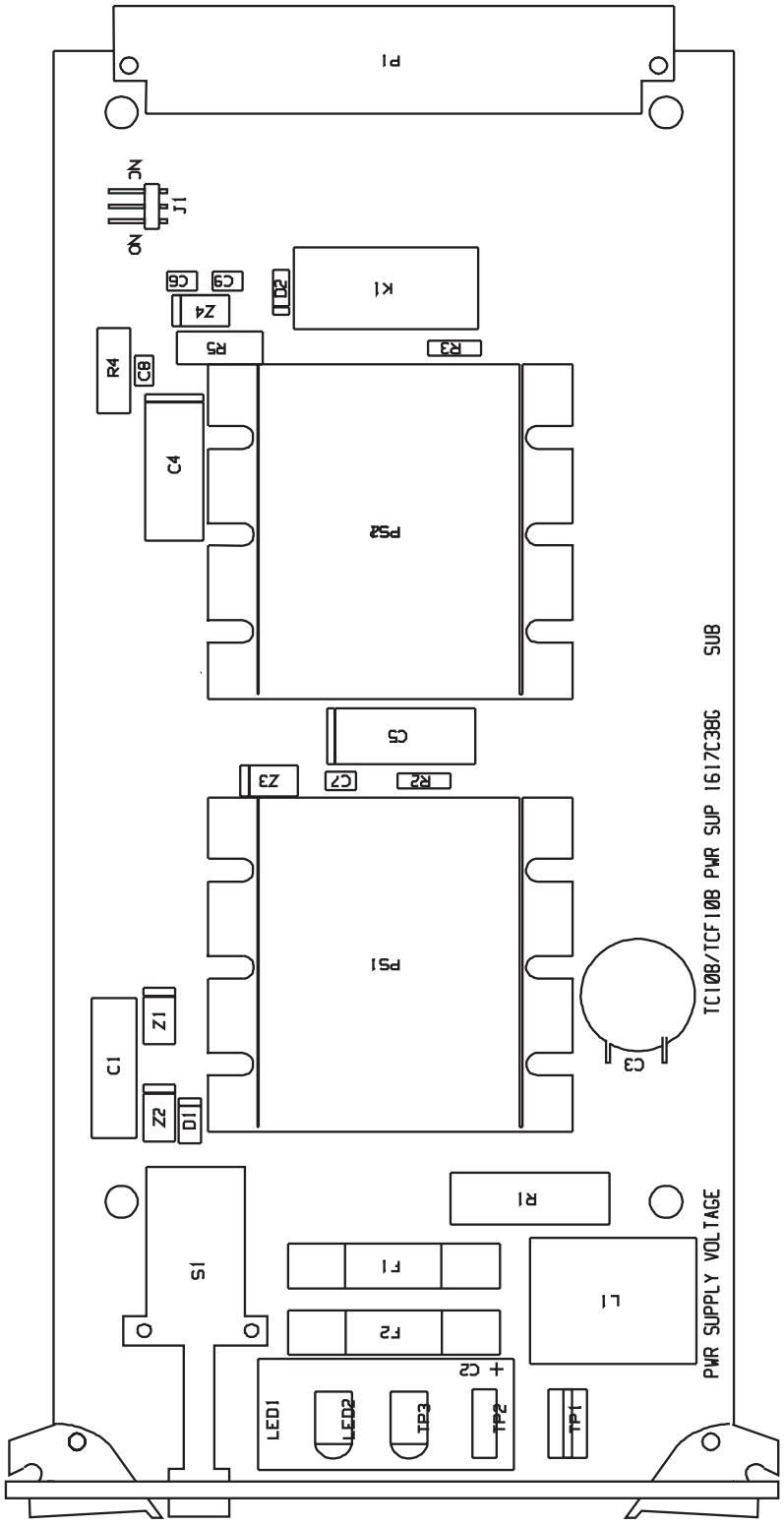


Figure 9–1. TC–10B/TCF–10B Power Supply Component Location (1617C38).

9.2 Power Supply Circuit Description

The module comprises the following circuits:

- Fuses
- ON/OFF Switch
- Input Filter
- Power Alarm Failure Relay
- dc/dc Converter (2)
- Output Filter

Fuses

	48V	125V	250V
F1, F2	3A	1.6A	3/4A

ON/OFF Switch

S1 - Pushbutton Switch (DPDT)

When in the "ON" position (pins 1 and 4), dc current flows through the input filter to the dc/dc converter.

Input Filter

The input filter (C1, C2, C3) contains zener diodes (Z1, Z2) that provide protection against surges, a diode (D1) that provides protection against reverse polarity, a differential choke XFMR (L1), and the Red Input LED1.

Power Alarm Failure Relay

This circuit includes:

- K1 - Alarm Relay
- J1 - Jumper (NO/NC)

Versions G04, G05, and G06 are without alarms.

In versions G01, G02, and G03 the field-selectable option can change the alarm contact de-energized state to NO or NC. (It is currently shipped in the NC de-energized state, and can be changed to NO if desired.)

DC/DC Converter

The two dc/dc converters (PS1 and PS2) operate at a maximum of 1 MHz and, as a result, switching noise is outside the 30-535 kHz range of the TC–10B/TCF–10B. The converter outputs, +20 Vdc and -20 Vdc, is fed to the output filter. (See Figure 9-1.)

Output Filter

The output filter for the +20 V consists of C4, C6, C8, and Z4. The output filter for the -20 V consists of C5, C7, C9, and Z3.

9.3 Power Supply Troubleshooting

The three test jacks on the control panel:

- TP3 (+20 Vdc)
- TP2 (Common)
- TP1 (-20 Vdc)

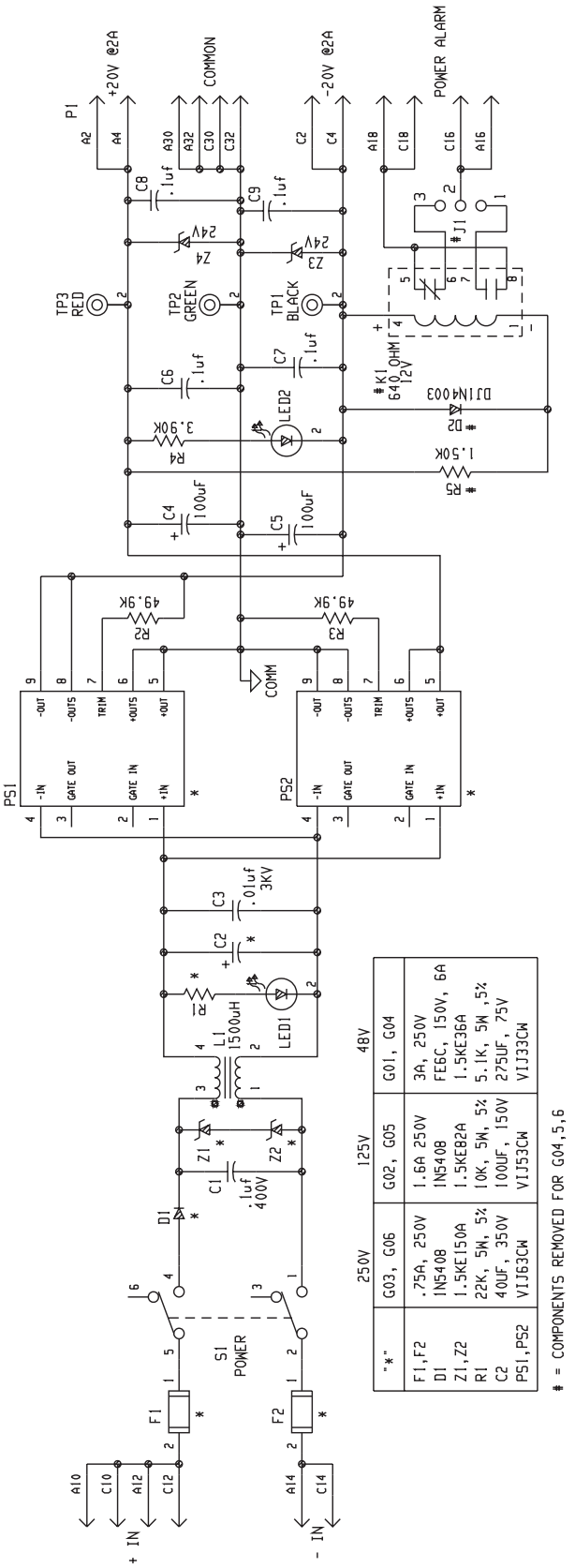
can be used to determine if the two voltages (+20 Vdc, -20 Vdc) are present. In addition, the LED2 output indicates that the dc/dc converters are generating voltage. The LED1 input indicates that voltage is present at the input of the dc/dc converter.

For basic troubleshooting, perform the following procedure:

1. If LED1 is not on with the module de-energized, remove and check the fuses (F1, F2) with an ohmmeter.
2. With the module de-energized, check the ON/OFF switch (S1) with an ohmmeter to be sure it opens and closes accordingly..
3. If LED2 is not on with the module energized, check the +20 V and -20 V outputs at TP3 and TP1, respectively. The one with voltage absent will require replacement of the associated dc/dc converter.

⚠ CAUTION

BE CAREFUL NOT TO MISPLACE SCREWS, SPRING WASHER OR INSULATING WASHER USED FOR MOUNTING TRANSISTORS.



	250V	125V	48V
"*"	G03, G06	G02, G05	G01, G04
F1,F2	.75A, 250V	1.6A 250V	3A, 250V
D1	1N5408	1N5408	FE6C, 150V, 6A
Z1,Z2	1.5KE150A	1.5KE82A	1.5KE36A
R1	22K, 5W, 5%	10K, 5W, 5%	5.1K, 5W ,5%
C2	40UF, 350V	100UF, 150V	275UF, 75V
PS1,PS2	VIJ63CW	VIJ53CW	VIJ33CW

Figure 9–2. TC–10B/TCF–10B Power Supply Schematic (1617C39).

Table 9–2. Power Supply Module Components (1617C38).

Location	Style	Description	Group
CAPACITORS			
C1	CE1003JU25	0.1 mF 5% 400 V MET POLYESTER	ALL
C2	CA10065N88	100 μF +150-10% 150 V ALUMINUM	02, 05
C2	CA27565K88	275 μF +150-10% 75 V ALUMINUM	01, 04
C2	CA40055T88	40 μF +150-10% 350 V ALUMINUM	03, 06
C3	CQ1002M3E4	.01 μF 3 KV CERAMIC DISC	ALL
C4,C5	CA10063E12	100 μF +75-10% 25 V ALUMINUM	ALL
C6, C7, C8, C9	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	ALL
CONNECTOR			
P1	9646A11H02	32-PIN RIGHT-ANGLE DIN CONNECTOR	ALL
CONVERTOR			
PS1, PS2	9658A45H01	VIJ53CW CONVERTOR	02, 05
PS1, PS2	9658A45H03	VIJ33CW CONVERTOR	01, 04
PS1, PS2	9658A45H02	VIJ63CW CONVERTOR	03, 06
DIODES			
D1	188A342H23	1N540B	02, 03, 05, 06
D1	3529A30H01	GI1303 150 V 6 A FAST	01, 04
D2	836A928H08	1N4007 1000 V 1 A	01, 02, 03
EJECTOR			
	1355D57H01		ALL
FUSE HOLDER			
	9644A50H01	FUSE CLIP	ALL
FUSES			
F1, F2	837A964H17	1.6 A 250 V 3 AG	02, 05
F1, F2	183A981H07	3 A 250 V 3 AG	01, 04
F1, F2	183A981H21	.75 A 250 V 3 AG	03, 06
HEADER			
J1	3533A56H05	3-POS 1-ROW RA HEADER (MAKE FROM 3533A56H06)	01, 02, 03
HEAT SINK			
	1606C65H06		ALL
INDUCTOR			
L1	3535A73H02	1,500 μH	ALL
JUMPER			
	3532A54H01	BLUE CLIP	01, 02, 03
LED			
LED1, LED2	3508A22H01	RED LED (EDGE MOUNT) 550-0406	ALL
PANEL			
	1616C46H05		ALL

Table 9–2. Power Supply Module Components (Cont'd).

Location	Style	Description	Group
RELAY			
K1	1484B33H01	1A1B 18.8 mA 12 V 640 OHMS	01, 02, 03
RESISTORS			
R1	RW1002J5G0	10 KILOHMS 5% 5 W WIREWOUND	02, 05
R1	RW5101J5G0	5.1 KILOHMS 5% 5 W WIREWOUND	01, 04
R1	RW2202J5G0	22 KILOHMS 5% 5 W WIREWOUND	03, 06
R2, R3	RM4992FQA9	49.9 KILOHMS 1% 0.25 W METAL FILM	ALL
R4	RC3901J167	3.9 KILOHMS 5% 1 W CARBON COMP	ALL
R5	RC1501J167	1.5 KILOHMS 5% 1 W CARBON COMP	01, 02, 03
ROLL PINS			
	9644A92H01	CONNECTOR	ALL
	9654A52H01	EJECTOR	ALL
SCREW			
	877A269H05	138-32 X .375 BND HD	ALL
SPACER			
R1	9640A72H01		ALL
STANDOFF			
	3537A39H06	138-32 X .5 PEMSERT	ALL
SWITCH			
S1	1444C63H06	DPDT ALT ACTION MECH INDICATOR	ALL
TEST JACKS			
TP1	3532A53H03	BLACK	ALL
TP2	3532A53H08	GREEN	ALL
TP3	3532A53H05	RED	ALL
WASHER			
	877A681H01	138 INTERNAL TOOTH	ALL
ZENERS			
Z1, Z2	878A619H10	1.5KE82A 82 V 5% 5 W 1.5 KW SURGE	02, 05
Z1, Z2	878A619H08	1.5KE36A 36 V 5% 5 W 1.5 KW SURGE	01, 04
Z1, Z2	878A619H06	1.5KE150A 150 V 5% 5 W 1.5 KV SURGE	03, 06
Z3, Z4	878A619H12	1.5KE24A 24 V 5% 5 W 1.5 KW SURGE	ALL

Chapter 10. Keying Module

Schematic	1606C29-7
Parts List	1606C29-7

Table 10–1. 1606C29 Styles and Descriptions.

Group	Description
G01	2- or 3-Frequency w/relay contacts

10.1 Keying Module Description

The TC–10B Keying Module controls the Transmitter Module as follows:

- Carrier Start (High-Level Test)
- Carrier Stop
- Low-Level Test
- Optional Checkback Test at High-Level (10 W)
- Optional Checkback Test at Low-Level (1 W)
- Optional Voice (4.3 W)

Keying Module outputs are as follows:

- High-Level (10 W)
- Voice (4.3 W)
- Any Transmitter Key (l W, l0 W, or Voice)

10.1.1 Keying Control Panel

(This panel is shown in Figure 1-1.)

Pushbutton Switches (recessed)

- High-Level (HL) Power (S1)
- Low-Level (LL) Power (S2)

LEDs for indicating Keying condition

- High-Level (10 W), Red (D10)
- Low-Level (1 W), Red (D11)
- Voice (4.3 W), Red (D12)

10.1.2 Keying PC Board Jumper Controls

(The Keying PC Board jumper controls are shown in Figure 10-1.)

JU1 Carrier Start 15 V, 48 V, 125 V, 250 V

JU2 Carrier Stop 15 V, 48 V, 125 V, 250 V

JU3 Low-Level Key 15 V, 48 V, 125 V, 250 V

JU7 Carrier Start/Stop Priority

JU6 Carrier Start NORM, INVERT

JU5 Carrier Stop NORM, INVERT

JU4 Low-Level Test NORM, INVERT

JU8 Carrier Stop (KA-4, SKBU-1)

10.2 Keying Circuit Description

The Keying Module (see Figure 10-2) provides an optically-isolated interface between the carrier and the relay system and controls the operation of the Transmitter Module with the following customer inputs:

- Carrier Start (High-Level Test)
- Carrier Stop
- Low-Level Test
- Optional Checkback Test at High-Level
- Optional Checkback Test at Low-Level
- Optional Voice

Keying Module outputs are as follows:

- High-Level (10 W)
- Any Transmitter Key
- Voice (4.3 W)

The logic blocks used are as follows:

- "AND" gate
- "OR" gate
- "Exclusive OR" gate
- "Inverter"

Logic "1" is +18.6 Vdc. Logic "0" is +3.6 Vdc. The following truth tables describe the operation of the building blocks.

AND	INPUTS		OUTPUTS
	A	B	Y
	0	0	0
	0	1	0
	1	0	0
	1	1	1

OR	INPUTS		OUTPUTS
	A	B	Y
	0	0	0
	1	0	1
	0	1	1
	1	1	1

Exclusive OR	INPUTS		OUTPUTS
	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0

INVERTER	INPUTS	OUTPUTS
	1	0
	0	1

Customer inputs operate as follows:

Carrier Start

When jumper JU6 is in the NORM position, carrier start will be initiated when the proper voltage level (15 V, 48 V, 125 V, or 250 V) is applied to pins A-10/C-10. When JU6 is in the INVERT position, carrier start will be initiated when voltage is removed from the input A/C-10.

> NOTE
>
> Carrier start will initiate a High-Level test.

Carrier Stop

When jumper JU5 is in the NORM position, carrier stop will initiate when jumper JU2 (pins A-16/C-16) is set at the appropriate voltage level (15 V, 48 V, 125 V, or 250 V); when JU5 is in the INVERT position, carrier stop will initiate when voltage is removed.

Low-Level Test

When jumper JU4 is in the NORM position, a Low-Level test will initiate when jumper JU3 (pins A-22/C-22) is set at the appropriate voltage level (15 V, 48 V, 125 V, or 250 V); when JU4 is in the INVERT position, a Low-Level test will initiate when voltage is removed.

When the appropriate jumper is in place on the board, jumpers JU1, JU2, and JU3 provide logic "1" or "0" inputs. (Proper polarity of these input commands must be observed.)

You can manually initiate a Low-Level test by pressing the (recessed) pushbutton switch (S2) on the front panel. You can manually initiate a High-Level test by pressing the (recessed) pushbutton switch (S1).

You can initiate an optional High-Level checkback key through pin C-8. You can initiate an optional Low-Level checkback key through pin C-28. A voice key can be initiated through pin C-24.

Keying Module outputs are as follows:

High-Level (10-W) Key	Pin A-8
Any Transmitter Key (1-W, 4.3-W, or l0-W)	Pin C-6
Voice (4.3-W) Key	Pin A-6

Front panel LEDs are illuminated as follows:

D10 High-Level

D11 Low-Level

D12 Voice

You can make the STOP command inhibit the High-Level (10 W) output by using jumper JU7. The STOP command also inhibits the Voice Key output. The Voice Key is inhibited by the High-Level and Low-Level Keys.

Zener diodes (D1, D2, D3) limit the input voltage to the optical isolators (I7, I8, I9), while also providing reverse voltage protection. Zener diodes (D14, D13) regulate primary power (pins A-2/A-4, pins A-30/A-32, pins C-30/C-32) down to 15 V, while also providing reverse voltage protection.

Transistor (Q1), JU8, R40, D15, D16, D17, and R41 are used for special applications with KDAR and SKBU type keying circuits. These particular relay applications have a single line input for carrier start. The line has a tri-state condition, i.e., it is active high, active low, or open circuit. For example, as shown in Figure 2-13 in the Applications chapter, under normal operating conditions, the input to TB4-1 is an open circuit (while looking back into Z1). CSB, CSP, and SQ are open, and zener diode (Z1) is much larger than 20 Vdc. When the carrier test switch is depressed, or the phase and ground carrier start contacts open, the line going to TB4-1 goes active high. If the phase and ground carrier stop contacts close, the line going to TB4-1 is active low.

As shown in the schematic of the keying load (Figure 10-2) and Q1 circuitry, when A-10 is high (same as TB4-1), carrier start is initiated and carrier stop is inhibited. This is caused by R40 and D15 saturating Q1 and shorting out the stop voltage applied to D7. C-16 is connected to the battery so that D2 ALWAYS has 20 V across it. When TB4-1 (A-10) goes active low, Diode D17 shorts out the drive voltage to Q1, and internal diode I8 conducts, causing a STOP function to be generated. The following TRUTH table illustrates the operation:

A10	CXR START	CXR STOP
HIGH	YES	NO
LOW	NO	YES
OPEN	NO	NO

When operating with systems other than KDAR or SKBU, normally J8 is left out, and three separate command lines (START, STOP, and LL) are used.

10.3 Keying Troubleshooting

Should a fault occur in the Keying Module, place the module on an extender board. Six jumpers (JU1 through JU6) are used to select input keying voltages and the sense required. A seventh jumper (JU7) governs start/stop priority. The three optical isolators (I7, I8, I9) may be tested using the on-board +18.6 Vdc source (D13 cathode). When a logic "1" is applied to any of the 15 V inputs (R4, R9, or R14), with the jumper removed, pin 5 of the selected optical isolator (I7, I8, or I9) will go low.

⚠ CAUTION

DO NOT ATTEMPT TO FORCE A LOGIC "1" (+18.6 VDC) ON ANY OUTPUTS OR INPUTS CONNECTED TO OUTPUTS. THIS COULD DAMAGE AN INTEGRATED CIRCUIT (IC).

You can check other components on the PC Board by conventional means.

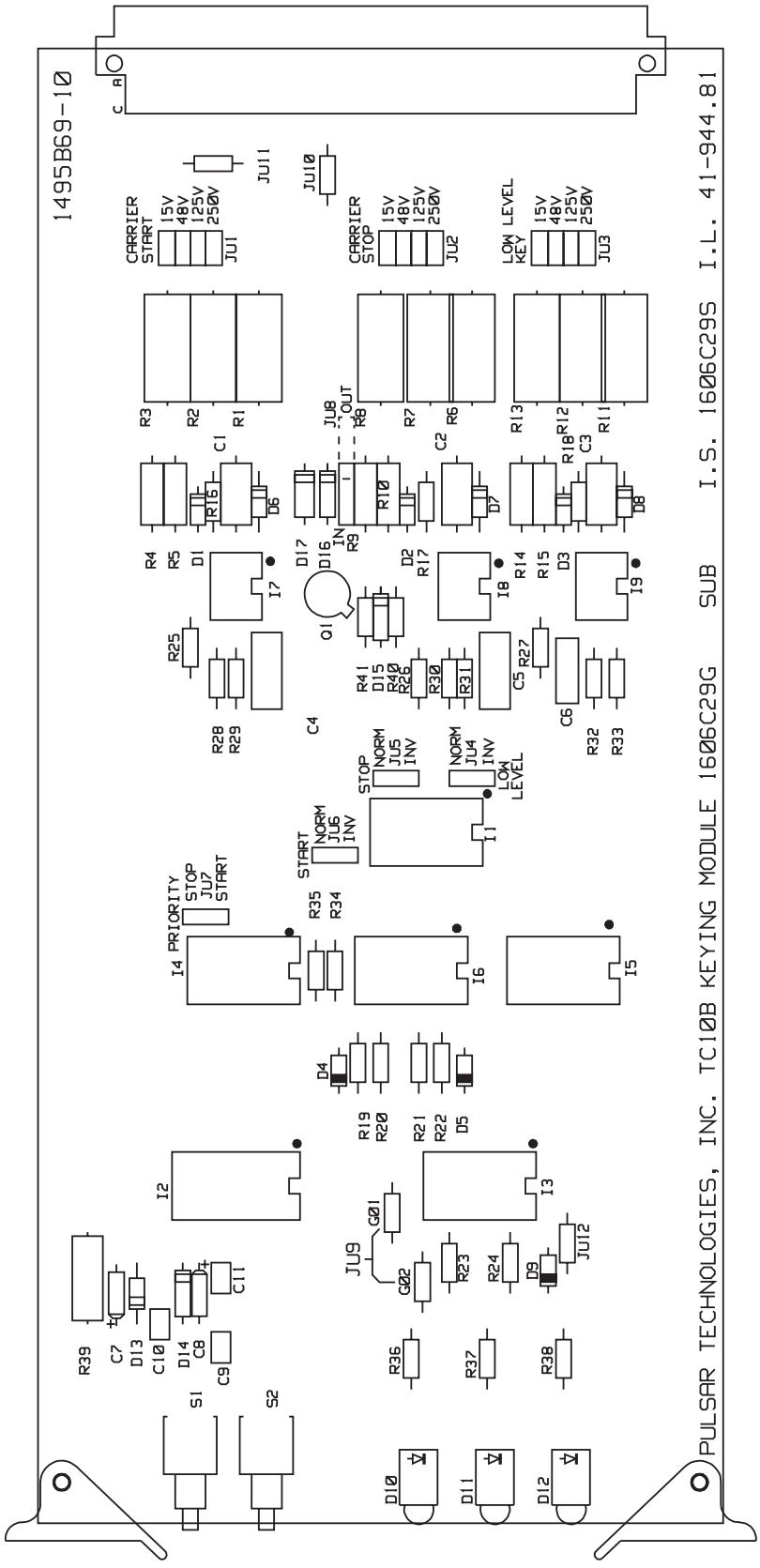


Figure 10–1. TC–10B Keying PC Board. (1495B69)

10

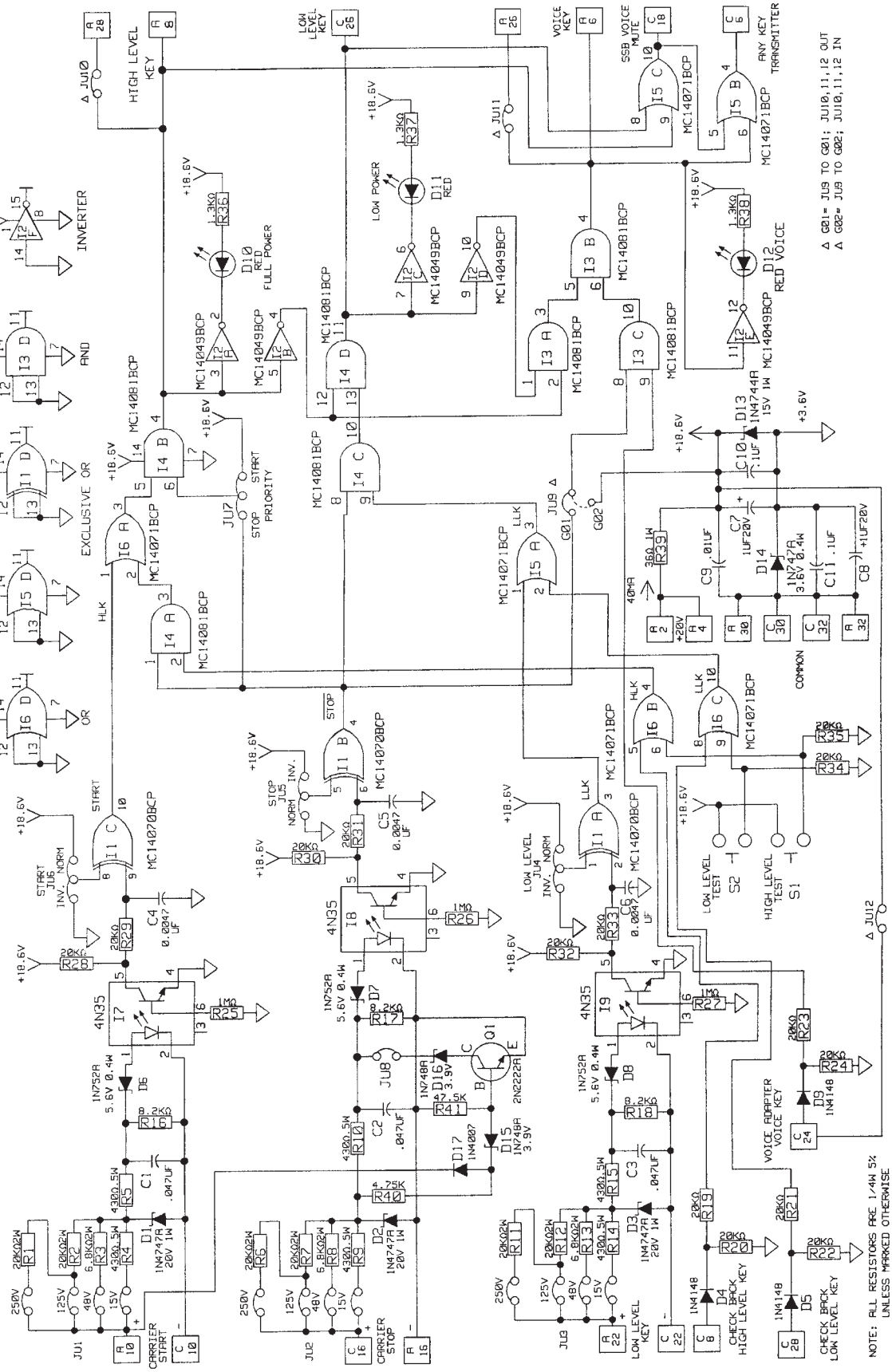


Figure 10–2. TC–10B Keying Schematic. (1606C29).

Table 10–2. Keying Module Components (1606C29).

Location	Style	Description	Group
CAPACITORS			
C01	CF4702JL78	0.047 μF 5% 100 V MET POLYCARB	01
C02	CF4702JL78	0.047 μF 5% 100 V MET POLYCARB	01
C03	CF4702JL78	0.047 μF 5% 100 V MET POLYCARB	01
C04	CT4701JW68	4,700 PF 5% 630 V MET POLYESTER	01
C05	CT4701JW68	4,700 PF 5% 630 V MET POLYESTER	01
C06	CT4701JW68	4,700 PF 5% 630 V MET POLYESTER	01
C07	CJ 1004MD72	1.0 μF 20% 20 V MOLDED TANTALUM	01
C08	CJ1004MD72	1.0 μF 20% 20 V MOLDED TANTALUM	01
C09	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C10	CPl 003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C11	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
DIGITAL ICs			
I01	3529A43H01	MC14070BCP QUAD EXCLUSIVE-OR	01
I02	3533A86H01	MC14049UBCP HEX INVERTER/BUFFER	01
I03	3536A17H01	MC14081BCP QUAD 2-INPUT AND	01
I04	3536A17H01	MC14081BCP QUAD 2-INPUT AND	01
I05	3536A15H01	MC14071BCP QUAD 2-INPUT OR	01
I06	3536A15H01	MC14071BCP QUAD 2-INPUT OR	01
DIODES			
D04	836A928H06	1N4148 75 V 0.01 A	01
D05	836A928H06	1N4148 75 V 0.01 A	01
D09	836A928H06	1N4148 75 V 0.01 A	01
D17	836A928H08	1N4007 I,000 V 1 A	01
JUMPERS			
JU01	3532A54H01	BLUE CLIP JUMPER	01
JU02	3532A54H01	BLUE CLIP JUMPER	01
JU03	3532A54H01	BLUE CLIP JUMPER	01
JU04	3532A54H01	BLUE CLIP JUMPER	01
JU05	3532A54H01	BLUE CLIP JUMPER	01
JU06	3532A54H01	BLUE CLIP JUMPER	01
JU07	3532A54H01	BLUE CLIP JUMPER	01
JU08	3532A54H02	PLUG IN	01
OPTOELECTRONICS			
D10	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01
D11	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01
D12	350BA22H01	RED LED (EDGE MOUNT) 550-0406	01
I07	774B936H01	4N35 OPTO-ISO.	01
I8	774B936H01	4N35 OPTO-ISO.	01
I9	774B936H01	4N35 OPTO-ISO.	01

(Continued on next page.)

Table 10-2. Keying Module Components (Cont'd).

Location	Style	Description	Group
RESISTORS			
R01	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R02	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R03	RC6801J249	6.8 KILOHMS 5% 2 W CARBON COMP	01
R04	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R05	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R06	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R07	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R08	RC6801J249	6.8 KILOHMS 5% 2 W CARBON COMP	01
R09	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R10	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R11	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R12	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R13	RC6801J249	6.8 KILOHMS 5% 2 W CARBON COMP	01
R14	RB4300JHL8	430 OHMS 50/o 0.5 W CARBON FILM	01
R15	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R16	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	01
R17	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	01
R18	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	01
R19	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R20	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R21	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R22	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R23	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R24	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R25	RB1 004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	01
R26	RBI 004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	01
R27	RBI 004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	01
R28	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R29	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R30	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R31	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R32	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R33	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R34	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R35	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	01
R36	RB1301JQB2	1.3 KILOHMS 5% 0.25 W CARBON FILM	01
R37	RB1301JQB2	1.3 KILOHMS 5% 0.25 W CARBON FILM	01
R38	RB1301JQB2	1.3 KILOHMS 5% 0.25 W CARBON FILM	01
R39	RC360AJ1E3	36 OHMS 5% 1 W CARBON COMP	01
R40	RM4751FQB0	4.75 KILOHMS 1% 0.25 W METAL FILM	01
R41	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01

Table 10-2. Keying Module Components (Cont'd).

Location	Style	Description	Group
SWITCHES			
S01	9646A57H01	SPST PUSH BUTTON	01
S02	9646A57H01	SPST PUSH BUTTON	01
TRANSISTORS			
Q01	762A672H15	2N2222A 40 V 0.8 A 0.4 W NPN	01
ZENERS			
D01	849A487H01	1N4747A 20 V 5% 1 W	01
D02	849A487H01	1N4747A 20 V 5% 1 W	01
D03	849A487H01	1N4747A 20 V 5% 1 W	01
D06	186A797H12	1N752A 5.6 V 5% 0.4 W	01
D07	186A797H12	1N752A 5.6 V 5% 0.4 W	01
D08	186A797H12	1N752A 5.6 V 5% 0.4 W	01
D13	849A515H04	1N4744A 15 V 5% 1 W	01
D14	837A398H08	1N747A 3.6 V 5% O.4 W	01
D15	186A797H13	1N748A 3.9 V 5% 0.4 W	01
D16	186A797H13	1N748A 3.9 V 5% 0.4 W	01

USER NOTES

Chapter 11. Transmitter Module

Schematic	1355D71-8
Parts List	1610C01-11

Table 11–1. 1610C01 Styles and Descriptions.

Group	Description
G01	TRANSMITTER 2- OR 3-FREQUENCY
G02	TRANSMITTER 2- OR 3-FREQUENCY W/TRANSFER TRIP TEST UNIT

11.1 Transmitter Module Description

The function of the TC–10B/TCF–10B Transmitter Module is to provide the RF signal which drives the 10W PA Module. The Transmitter's frequency range is from 30 kHz to 535 kHz, programmable in 0.1 kHz (100 Hz) steps by four rotary switches on the Transmitter. The Transmitter is slaved to a crystal oscillator.

The TC–10B/TCF–10B Transmitter Module operates from keyed inputs (set by jumpers at the Keying Module):

- High-Level Key
- Any Transmitter Key
- Voice Key
- Shift High (TCF–10B only)
- Shift Low (TCF–10B only)

The Transmitter Module also operates with a signal from the Optional Voice Adapter Module:

- AM Voice

The Transmitter Module operates with either no shift or one of three different frequency shifts, selectable by a four-position dip switch (S5).

11.1.1 Transmitter Control Panel

(This panel is shown in Figure 1-1.)

Operator controls consist of four thumbwheel switches (with indicator windows), representing the frequency range:

- SW1 (x 100 kHz)
- SW2 (x 10 kHz)
- SW3 (x 1 kHz)
- SW4 (x 0.1 kHz)

After pulling the module, use a screw driver to set the thumbwheel switches: CW for higher frequency, CCW for lower frequency.

11.1.2 Transmitter PC Board

(The Transmitter PC Board is shown in Figure 11-1.)

Operator controls are as described below.

Potentiometers

R13 Adjusts high-level (10 W) output

R12 Adjusts low-level (1 W) output

R14 Adjusts voice (4.3 W) output level

R1 Adjusts modulation of transmitter signal (peak-to-valley ratio of signal envelope)

R29 Sets the offset in output amplifier, so that when 0 dBm is generated, R29 is adjusted to minimize the 2nd harmonic distortion

Capacitor

C19 Adjustment for 3.27680 MHz clock oscillator

Switch

S5 Frequency-shift select

Test Point

TP1 Clock Oscillator Output

11.2 TRANSMITTER CIRCUIT DESCRIPTION

The function of the Transmitter Module (see Figure 11-2, Schematic 1355D71) is to provide the RF signal (0 dBm/.001W, 50 ohm balanced), which drives the 10W PA Module. The Transmitters frequency range is from 30 kHz to 535 kHz, programmable in 0.1 kHz (100 Hz) steps by four rotary switches on the Transmitter. The Transmitter Module operates from keyed inputs (set by jumpers at the Keying Module):

- High-Level (10W) Key (pins C/A-8)
- Any Transmitter Key (pin A-10)
- Voice Key (pins C/A-6)
- Shift High (pin C-10) (TCF–10B Only)
- Shift Low (pins A/C 24) (TCF–10B Only)

The Transmitter Module also operates from an audio signal from the Optional Voice Adapter Module: AM Voice (pins C/A-26). Refer to Figure 11-3, Transmitter Block Diagram.

Frequencies are selected using the four BCD (Binary Coded Decimal) switches (SW1 thru SW4); the range is from 30.0 to 535.0 kHz, in 0.1 kHz (100 Hz) steps. The 15-bit output of the BCD switches is converted to a 13-bit binary number by the BCD-to-Binary converter (ROMs I1 and I2).

The 13-bit output of ROMs I1 and I2 provides an input to the Shift and Control Logic (I3), which consists of three parts:

1. A full adder/subtracter which functions under control of:
   - Shift High (Add)
   - Shift Low (Subtract)
2. A frequency-shift, in 50 Hz increments from 0 to 750 Hz, selected by the 4-position dip-switch (S5).
3. A sequencer and multiplexer (MUX) which provides the following outputs to the Numerical Controlled Oscillator (NCO I4):
   - Address select (ADDR)
   - Write (WRN)
   - Load (LDSTB)
   - 2 (8-bit sequential) data bytes

The NCO (I4) generates digital sine functions of very precise frequency, to be used in conjunction with a D/A converter (I5) in analog frequency generation applications. The NCO is designed to interface with and be controlled from an 8-bit bus.

The NCO maintains a record of phase which is accurate to 16 bits. At each clock cycle, the number stored in the 16-bit phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine function. The number in the Δ-phase register represents the change of phase for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_0 = \frac{f_C \times \Delta\text{-phase}}{2^{16}}$$

where: f_0 is the frequency of the output signal

and: f_C is the clock frequency (3.27680 MHz)

The sine function is generated from the 13 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ-phase register, which may be programmed by two sequential 8-bit inputs.

The frequency programming capability of the NCO is analogous to sampling a sine wave where the sampling function is the clock.

If the output frequency is very low with respect to the clock (less than f_C / 8096), then the NCO output will sequence through each of the 8096 states of the sine function. As the output frequency is increased with respect to the clock, the sine function will appear to be more discontinuous, because there will be fewer samples in each cycle. At the Nyquist limit, when the output frequency is exactly half the clock, the output waveform reduces to a square wave. The practical upper limit of the NCO output frequency is about 40% of the clock frequency because spurious components created by sampling, which are at a frequency greater than half-the-clock frequency, become difficult to remove by filtering.

The 12-bit output of the NCO is applied to the input of the high-speed Digital-to-Analog Converter (I5), which converts a digital sine wave from the NCO to an analog output. The analog output from I5 is filtered by a 630 kHz Low Pass Filter (C14, C13, L1, L2, C15), producing a 0.512 Vp-p output at the carrier frequency. The carrier frequency is applied to Modulator (I7), where it is modulated by a dc and/or ac signal from a 2 kHz Low Pass Filter (I10, R24, R25, R26, C30, C31, C32). The output of I7 drives the Output Amplifier (I11) and associated components. The output of I11 is coupled through the Output Transformer (T1) to provide a 50 ohm balanced output.

The reference frequency to the NCO is generated by a Crystal-Controlled Clock Oscillator (CCCO), consisting of Y1, CMOS inverter (I6A), R3, R4, C19, C20, and C50, at a frequency of 3.27680 MHz. The CCCO is buffered by I6B, which drives the Shift and Control Logic (I3) and the NCO clocks. The modulator (I7) receives its inputs from the Analog MUX (I9) used for modulation selection, through the Low Pass Filter whose functions are described (in paragraphs 11.2.1, 11.2.2 and 11.2.3) below.

11.2.1 Low-Level Operation

When Transmitter key input voltage (pin A10) is present, it removes the reset from the NCO (I4). If no other input voltage is present (Transmitter key signal only), the voltage divider (R12, R10) supplies the modulating voltage to the modulator (I7), through the selected analog multiplexer (I9) channel. The 1 watt low-level operation is produced when I9 (both A and B) are either “0” or “1”, causing I9 to connect inputs X0 and Y0, or X3 and Y3 to the outputs X and Y. Potentiometer R12 controls the low-level output, which is between 0 and 1 mW.

11.2.2 High-Level Operation

When the 10W voltage is keyed, it produces a “1” at the I9 B input, causing channel 2 to be selected. If no other input voltage is present (10 W key signal only), the voltage divider (R10, R13) supplies the modulating voltage to the modulator (I7) through the multiplexer (I9) channel.

The 10 watt high-level operation is produced when I9 A input is “0” and I9 B input is “1”, causing I9 to connect inputs X2 and Y2 to the output X and Y. Potentiometer R13 controls the high-level output, which is between 0 and 1 mW.

11.2.3 Voice Operation

When the Voice key input voltage is present, it produces a “1” at I9A input, causing channel 1 to be selected. If no other input voltage is present (Voice key signal only), the voltage divider (R10, R14) supplies the modulating voltage to the modulator (I7), through the selected analog multiplexer (I9) channel. The Voice operation is produced when I9 A input is “1” and I9 B input is “0”, causing I9 to connect X1 and Y1 to the outputs X and Y. Potentiometer R14 controls the voice carrier output level of the AM carrier, which is between 0 and 1 mW. In addition, an ac signal from AM Voice Input is added to the dc level (through R8, R11, and C26) to modulate the carrier. The audio modulating level is adjusted (by potentiometer R11) to a maximum of 60% modulation.

On-board voltage regulation is provided by voltage regulators I8 (+5 V), I12 (+15 V), I13 (-15 V) and associated components. The circuitry operates at +15 V, +5 V, or -15 V. All bypassing is to common or PC Board ground. Additional regulated voltages of +4.3 V and -4.3 V are generated by I7 to provide an extremely stable reference for modulating control voltages (provided by R12, R13, and R14).

11.2.4 Frequency-Shift Operation (TCF–10B only)

For TCF–10B operation, circuitry is provided to shift the frequency of the NCO (I4), which supplies the modulator (I7). Shift-low and shift-high commands are fed from the Keying Module to connector pins C/A-24 and C-10, respectively. The NCO can operate on three different frequencies, depending on the combination of shift-high and shift-low inputs to the Shift and Control Logic (I3).

The **shift-low** command causes I3 to select the shift frequency voltage from the Frequency Shift Selector Switch (S5). The NCO (I4) output shifts to a lower frequency and the Transmitter output shifts to a lower frequency ($f_C - f_{shift}$).

The **shift-high** command causes I3 to select the shift frequency from the Frequency Shift Selector (S5). The NCO (I4) output shifts to a higher frequency and the Transmitter output shifts to a higher frequency ($f_C + f_{shift}$). The operation of this command is similar to that of the shift-low command, except that the shift is added to (rather than subtracted from) the carrier frequency.

When there is no command to shift low or high, both SL and SH inputs to I3 are logic “1”, and no shift is added to the carrier frequency.

11.3 Transmitter Troubleshooting

Should a fault occur in this module, place the module on an extender board. Check the RF output (30 to 535 kHz) on pins A/C-28. If there is a Voice Key or AM voice input, use an oscilloscope to examine the modulation envelope. You can check the ac and dc voltages provided on the schematic (Figure 11-2) at the appropriate points, for the conditions on the schematic (10 W, 1 W, and Voice).

You can check all diodes, resistors, chokes and transistors by conventional means.

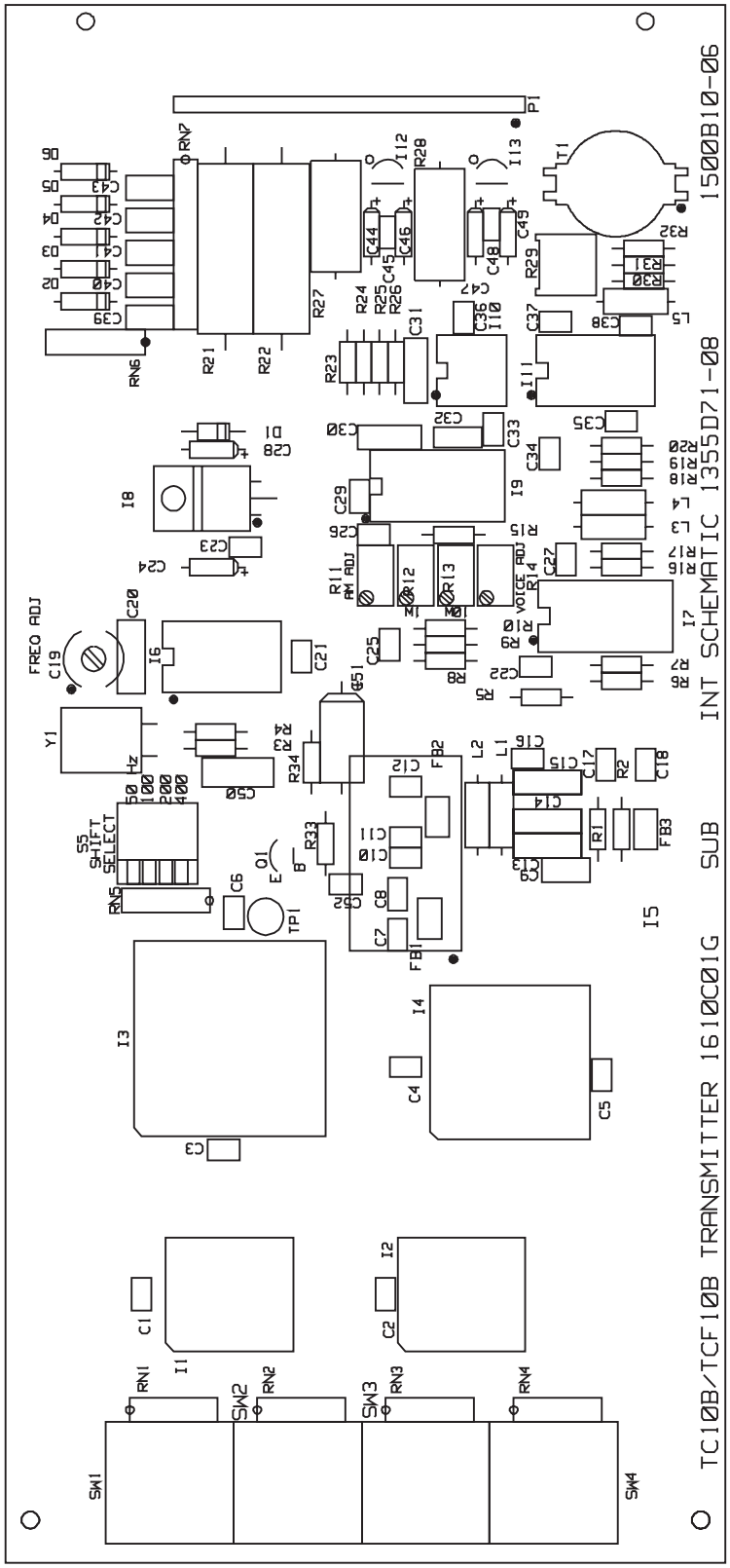


Figure 11–1. TC–10B/TCF–10B Transmitter PC Board (1500B10).

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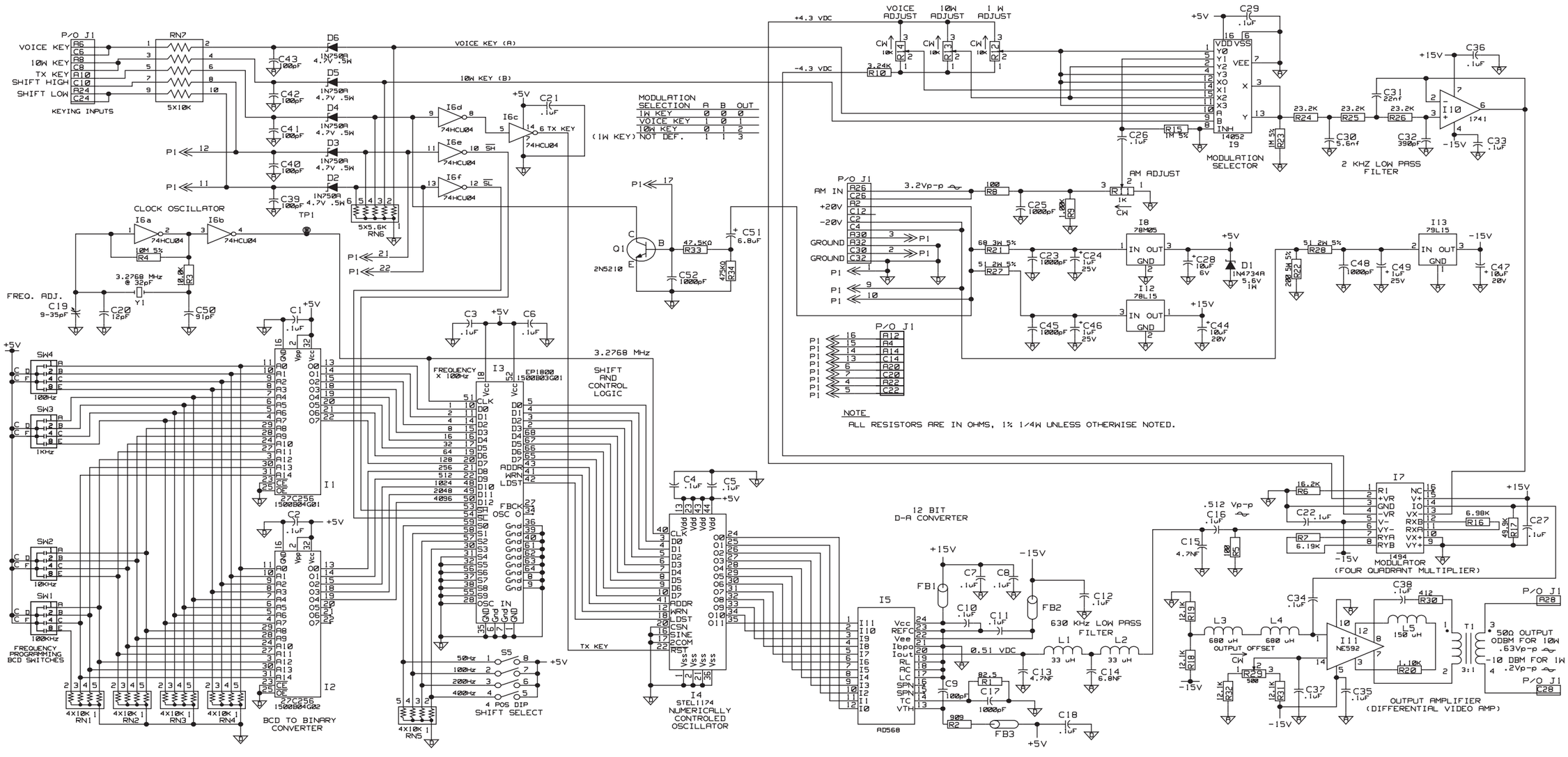

Figure 11–2. TC–10B Transmitter Schematic (1355D71).

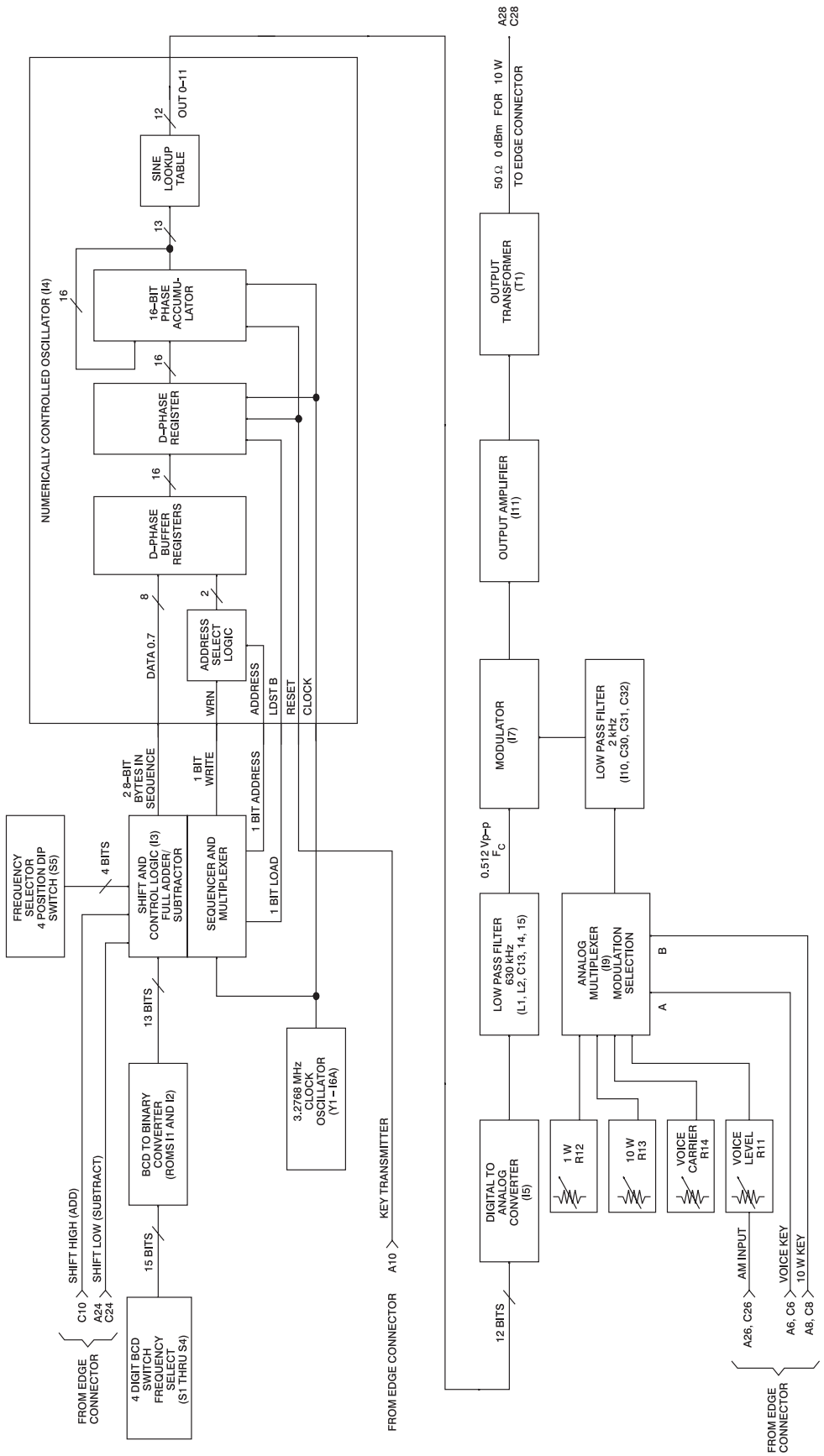

Figure 11–3. TC–10B Transmitter Block Diagram (1610C09).

Table 11–2. Transmitter Module Components (1610C01).

Location	Style	Description	Group
BEADS			
FB1	9651A21H01	FERRITE BEADS	01
FB2	9651A21H01	FERRITE BEADS	01
FB3	9651A21H01	FERRITE BEADS	01
CAPACITORS			
C1	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C2	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C3	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C4	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C5	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C6	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C7	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C8	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C9	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C10	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C11	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C12	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C13	CT4701JW68	4,700 pF 5% 630 V MET POLYESTER	01
C14	CT6801JW68	6,800 pF 5% 630 V MET POLYESTER	01
C15	CT4701JW68	4,700 pF 5% 630 V MET POLYESTER	01
C17	CP1001ML65	1,000 pF 20% 100 V X7R MONO CERAMIC	01
C20	CR180AGV92	18 pF 2% 500 V DIPPED MICA	01
C23	CP1001ML65	1,000 pF 20% 100 V X7R MONO CERAMIC	01
C24	CJ1004MD72	1.0 µF 20% 20 V MOLDED TANTALUM	01
C25	CP1001ML65	1,000 pF 20% 100 V X7R MONO CERAMIC	01
C28	CJ1005MA72	10 µF 20% 6 V MOLDED TANTALUM	01
C30	CT5601JU74	5,600 pF 5% 400 V MET POLYESTER	01
C31	CT2202JQ74	0.022 µF 5% 250 V MET POLYESTER	01
C32	CR3900JH67	390 pF 5% 50 V DIPPED MICA	01
C39	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C40	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C41	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C42	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C43	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C44	CJ1005MD72	10 µF 20% 20 V MOLDED TANTALUM	01
C45	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	01
C46	CJ1004MD72	1.0 µF 20% 20 V MOLDED TANTALUM	01
C47	CJ1005MD72	10 µF 20% 20 V MOLDED TANTALUM	01
C48	CP1001ML65	1,000 pF 20% 100 V X7R MONO CERAMIC	01
C49	CJ1004MD72	1.0 µF 20% 20 V MOLDED TANTALUM	01
C50	CR910AGVA6	91 pF 2% 500 V DIPPED MICA	01
C51	CJ6804MG72	6.8 µF 20% 35 V MOLDED TANTALUM	01
C52	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01

Table 11–2. Transmitter Module Components (Cont'd).

Location	Style	Description	Group
CHOKES			
L1	9646A07H31	33.0 μH	01
L2	9646A07H31	33.0 μH	01
L3	9646A07H47	680.0 μH	01
L4	9646A07H47	680.0 μH	01
L5	9646A07H39	150.0 μH	01
DIGITAL ICS			
I9	9646A33H01	MC14052BCP DUAL 4-CHAN ANALOG MUX	01
EPROMS			
I1	1500B04G01	ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY	01
I2	1500B04G02	ELECTRICALLY PROGRAMMABLE READ- ONLY MEMORY	01
INT CKTS			
I3	1500B03G01	ELECTRICALLY PROGRAMMABLE LOGIC DEVICE	01
I4	9651A22H01	STEL 1174 NCO (44PIN)	01
I5	9651A19H01	AD568 D/A CONVERTER	01
I6	9651A18H01	74HCU04N HEX UNBUF F INV	01
I7	9651A16H01	MC1494L	01
LINEAR ICS			
I10	6277D61H10	MC1741U SINGLE OP-AMP	01
I11	9646A35H01	NE592N WIDEBAND VIDEO AMP	01
I12	9648A02H05	MC78L15ACP POS VOLTREG 15 V 5% 0.1 A	01
I13	9648A82H03	MC79L15ACP NEG VOLTREG 15 V 5% 0.1 A	01
I8	9651A15H01	MC78M05CT	01
POTENTIOMETERS			
R11	3534A25H04	1K 25T TOP ADJ.	01
R12	3534A25H07	10K 25T TOP ADJ	01
R13	3534A25H07	10K 25T TOP ADJ	01
R14	3534A25H07	10K 25T TOP ADJ	01
R29	3502A17H08	500-OHM .5 W 1 TURN CERMET TOP ADJ.	01
RESISTOR NETWORKS			
RN1	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	01
RN2	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	01
RN3	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	01
RN4	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	01
RN5	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	01

(Continued on next page.)

Table 11–2. Transmitter Module Components (Cont'd).

Location	Style	Description	Group
RESISTORS			
R1	RM825AFQB4	82.5 OHMS 1% 0.25 W METAL FILM	01
R10	RM3241FQB0	3.24 KILOHMS 1% 0.25 W METAL FILM	01
R15	RM1004FQ99	1.00 MEGOHMS 1% 0.25 W METAL FILM	01
R16	RM6981FQB0	6.98 KILOHMS 1% 0.25 W METAL FILM	01
R17	RM4992FQA9	49.9 KILOHMS 1% 0.25 W METAL FILM	01
R18	RM1212FQA9	12.1 KILOHMS 1% 0.25 W METAL FILM	01
R19	RM1212FQA9	12.1 KILOHMS 1% 0.25 W METAL FILM	01
R2	RM9090FQB1	909 OHMS 1% 0.25 W METAL FILM	01
R20	RM1101FQB0	1.10 KILOHMS 1% 0.25 W METAL FILM	01
R21	RW910AJ5G0	91 OHM 5 W 5% WIRE WOUND	01
R22	RW2000J5G0	200 OHMS 5% 5 W WIREWOUND	01
R23	RM1004FQ99	1.00 MEGOHMS 1% 0.25 W METAL FILM	01
R24	RM2322FQA9	23.2 KILOHMS 1% 0.25 W METAL FILM	01
R25	RM2322FQA9	23.2 KILOHMS 1% 0.25 W METAL FILM	01
R26	RM2322FQA9	23.2 KILOHMS 1% 0.25 W METAL FILM	01
R27	RC510AJ269	51 OHMS 5% 2 W CARBON COMP	01
R28	RC510AJ269	51 OHMS 5% 2 W CARBON COMP	01
R3	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R30	RM4120FQB1	412 OHMS 1% 0.25 W METAL FILM	01
R31	RM1212FQA9	12.1 KILOHMS 1% 0.25 W METAL FILM	01
R32	RM1212FQA9	12.1 KILOHMS 1% 0.25 W METAL FILM	01
R33	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R34	RM4753FQ98	475 KILOHMS 1% 0.25 W METAL FILM	01
R4	RB1005JQB3	10 MEGOHMS 5% 0.25 W CARBON FILM	01
R5	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01
R6	RM1622FQA9	16.2 KILOHMS 1% 0.25 W METAL FILM	01
R7	RM6191FQB0	6.19 KILOHMS 1% 0.25 W METAL FILM	01
R8	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01
R9	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	01
CRYSTAL			
Y1	9651A68H01	3.27680 MHz HC18/U 10PPM	01
SWITCHES			
SW1	3533A83H03	THUMBWHEEL BCD 5 POS.	01
SW2	3533A83H02	THUMBWHEEL BCD 10 POS.	01
SW3	3533A83H02	THUMBWHEEL BCD 10 POS.	01
SW4	3533A83H02	THUMBWHEEL BCD 10 POS.	01
SW5	775B517H04	4 POS DIP	01
TRANSFORMERS			
T1	1487B55H01	660-OHM: 75-OHM INTERSTAGE W.B.	01

Table 11–2. Transmitter Module Components (Cont'd).

Location	Style	Description	Group
TRANSISTORS			
Q1	3509A35H12	2N5210 50 V 0.05 A 1.0 W NPN	01
TRIMMERS			
C19	879A834H01	5.5-18 pF TRIMMER	01
ZENERS			
D1	849A515H13	1N4734A 5.6 V 5% 0.4 W	01
D2	837A398H03	1N750A 4.7 V 5% 0.4 W	01
D3	837A398H03	1N750A 4.7 V 5% 0.4 W	01
D4	837A398H03	1N750A 4.7 V 5% 0.4 W	01
D5	837A398H03	1N750A 4.7 V 5% 0.4 W	01
D6	837A398H03	1N750A 4.7 V 5% 0.4 W	01

USER NOTES

Chapter 12. 10W PA Module

Schematic	1606C33-20
Part List	1606C33-20

Table 12–1. 1606C33 Styles and Descriptions.

Group	Description
G01	WITH POWER ON RELAY
G02	WITHOUT POWER ON RELAY

12.1 10W PA Module Description

The function of the TC–10B/TCF–10B 10 W PA Module is to amplify a 0 dBm (1 mW) input to an output power level of 10 W. You may also adjust the 10W PA for input power levels from 0.5 mW to 2 mW.

The 10W PA Module operates in a 30 to 535 kHz range without tuning. The amplifier has a fixed gain of approximately 49 dB (class A, complementary symmetry push-pull stage). Negative feedback is used to derive a nominal output impedance of 50 ohms.

12.1.1 10W PA Control Panel

(This panel is shown in Figure 1–1.)

Operator controls are as Described below.

Potentiometer (R53) INPUT LEVEL SET

Adjusts power output level to 10 W with 1 mW input.

LED, TRANSMIT, RF Power Indication, Red (D6)

Test Jacks

- INPUT (TJ1)
- COMMON (TJ2)

Optional relay alarm for RF voltage

12.1.2 10W PA PC Board

(The 10W PA PC Board is shown in Figure 12-1.)

Operator controls consist of a Jumper (JU1) for the Alarm Relay (NO/NC), which indicates loss of power condition (less than 1 W).

12.2 10W PA Circuit Description

The function of the 10W PA Module (see Figure 12-2, Schematic 1606C33S) is to amplify a 0 dBm (1 mW) input to an output power level of 10 W. The input from pins C28/A28 passes thru a 700 kHz low pass filter (LPF) consisting of L1 and C1. Potentiometer (R53), labeled "INPUT LEVEL SET" on the front panel, is used to adjust the power level to 10 W output with 1 mW applied at the input.

The 10W PA Module operates in a 30 to 535 kHz range without tuning. The amplifier has a maximum gain of approximately 49 dB (class A, complementary symmetry push-pull stage). Negative feedback is used to derive a nominal output impedance of 50 ohms.

All bypassing is done to common (pins A30/C30, A32/C32). Transistors QN1, QN2 and QN3 are 14 pin DIPs, each containing four individual transistors; QN1 is PNP, while QN2 and QN3 are NPN.

The LPF output drives the amplifier QN1 and QN2. QN1A/QN1B and QN2A/QN2B are configured as a differential amplifier, while QN1C and QN2C are constant current sources. The input

signal is applied to the bases of QN1A and QN2A. Negative feedback is applied to the bases of QN1B and QN2B. At the positive side (QN2), the differential output from QN2A and QN2B is amplified by QN2D and Q2. At the negative side (QN1), the differential output from QN1A and QN1B is amplified by QN1D and Q1. The positive side power output transistor (Q6) is driven by Q5; the negative side power output transistor (Q7) is driven by Q4.

The no-load feedback is from transformer (T1) back thru the RC network of R21, C7, C2, C5 and R18 to the junction of R16 and R17, for the purpose of stability. The loaded feedback is derived from a sampling resistor (R33, R35, R36, R37, R38, and R39, all in parallel) and fed back thru C28, C29 and R23. The overall no-load voltage gain is approximately 282. The overall loaded voltage gain is approximately 141. The partial loaded gain, between C28/A28 and the primary of T1, is approximately 38.

The alarm circuit (loss of RF signal condition) consists of QN3, Q8, K1 and associated components. The RF signal is monitored by C22, at T1 pin 1. The signal sample is amplified in QN3A and fed to QN3B and QN3C (QN3B and QN3C are configured as diodes). A voltage doubler is formed from C30, QN3C and QN3B. The output of QN3B drives QN3D, via R44 and R45. QN3D is saturated for an input of 1 W to C22 (with reference to T1 secondary). As QN3D saturates, Q8 conducts, driving the front panel LED (D6, power monitor), causing K1 to energize (or de-energize), indicating loss of signal condition. Jumper JU1 allows the selection of an open circuit or a closed circuit for the loss of signal condition.

The +20 Vdc line (leading to the alarm circuit, etc.) is filtered by C10, C11, L2, L4, C19, C20 and C21. The -20 Vdc (leading to C2/C4) is filtered by C12, C13, L3, C16, C17, C18 and L5.

12.3 10W PA Troubleshooting

To check individual transistors, e.g., Q1 thru Q8, QN1, QN2 and QN3, remove them first from the PC Board. Ohmmeter measurements of the transistors while in the PC Board are misleading because of other paths on the board.

You may remove the heat sink by unscrewing the four (4) corner screws and the hold-down screws for Q1 thru Q8. The 10W PA Module can operate at no-load conditions without the heat sink for short periods of time while you are troubleshooting.

⚠ CAUTION

THE 10W PA IS, BASICALLY, AN OP-AMP PROVIDING VERY HIGH GAIN WITH NEGATIVE FEEDBACK. TRANSISTORS Q1 THROUGH Q5, Q6, AND Q7 ARE THERMALLY CONNECTED, I.E., THEY ARE MOUNTED ON THE SAME PART OF THE HEAT SINK. ANY FAILING TRANSISTOR MAY AFFECT OTHER TRANSISTORS. CHECK EACH TRANSISTOR SEPARATELY. IF NO FAULTS ARE FOUND, CHECK OTHER COMPONENTS.

BE CAREFUL NOT TO MISPLACE THE SCREWS, SPRING WASHER OR INSULATING WASHER USED TO MOUNT Q1 THROUGH Q8. DAMAGED SCREWS OR INSULATORS SHOULD NOT BE USED.

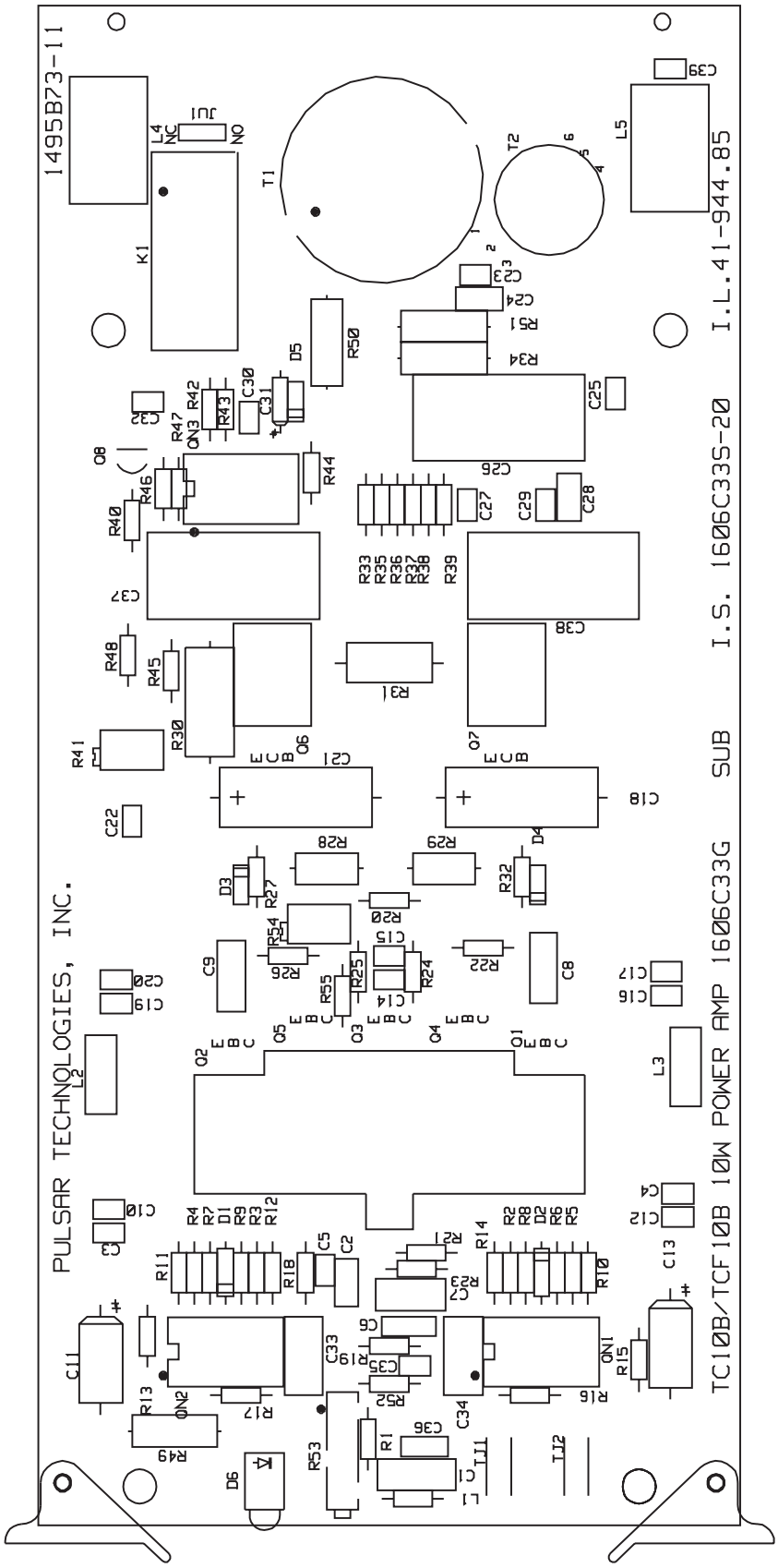

Figure 12–1. TC–10B/TCF–10B 10W PA PC Board (1495B73; Sheet 5 of 7).

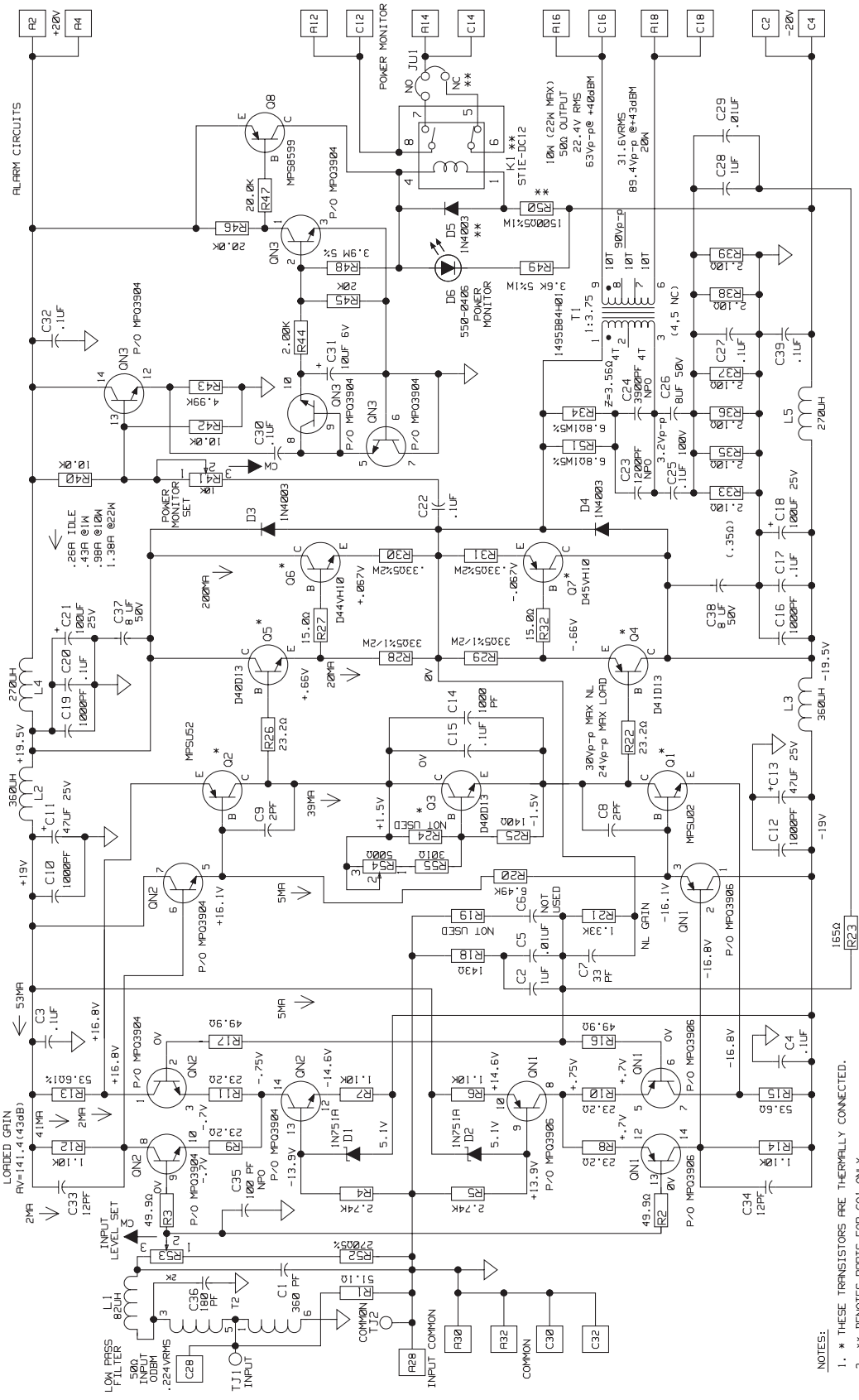

Figure 12–2. 10W PA Schematic (1606C33).

Table 12–2. 10W Power Amplifier Components (1606C33).

Location	Style	Description	Group
CAPACITORS			
C01	CR3900GV91	390 pF 2% 500 V DIPPED MICA	01,02
C02	CP1004MH54	1.0 μF 20% 50 V MONO CERAMIC	01,02
C03	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C04	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C05	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01,02
C07	CR330AGV92	33 pF 2% 500 V DIPPED MICA	01,02
C08	CR200BDV67	2 pF +/-0.5pF 500 V DIPPED MICA	01,02
C09	CR200BDV67	2 pF +/-0.5pF 500 V DIPPED MICA	01,02
C10	CP1001GH65	1,000 pF 2% 50 V C0G MONO CERAMIC	01,02
C11	CJ4705ME72	47 μF 20% 25 V MOLDED TANTALUM	01,02
C12	CP1001GH65	1,000 pF 2% 50 V C0G MONO CERAMIC	01,02
C13	CJ4705ME72	47 μF 20% 25 V MOLDED TANTALUM	01,02
C14	CP1001GH65	1,000 pF 2% 50 V C0G MONO CERAMIC	01,02
C15	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C16	CP1001GH65	1,000 pF 2% 50 V C0G MONO CERAMIC	01,02
C17	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C18	CA10063E12	100 μF +75-10% 25 V ALUMINUM	01,02
C19	CP1001GH65	1,000 pF 2% 50 V C0G MONO CERAMIC	01,02
C20	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C21	CA10063E12	100 μF +75-10% 25 V ALUMINUM	01,02
C22	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C23	CP1201GL65	1,200 pF 2% 100 V C0G MONO CERAMIC	01,02
C24	CP3901GH65	3,900 pF 2% 50 V C0G MONO CERAMIC	01,02
C25	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C26	CE8004JH64	8.0 μF 5% 50 V MET POLYCARBONATE	01,02
C27	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C28	CP1004MH54	1.0 μF 20% 50 V MONO CERAMIC	01,02
C29	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01,02
C30	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C31	CJ1005MA72	10 μF 20% 6 V MOLDED TANTALUM	01,02
C32	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02
C33	CR120AJV67	12 pF 5% 500 V DIPPED MICA	01,02
C34	CR120AJV67	12 pF 5% 500 V DIPPED MICA	01,02
C35	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	01,02
C36	CR3900JH67	390 pF 5% 50 V DIPPED MICA	01,02
C37	CE8004JH64	8.0 μF 5% 50 V MET POLYCARBONATE	01,02
C38	CE8004JH64	8.0 μF 5% 50 V MET POLYCARBONATE	01,02
C39	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02

(Continued on next page.)

Table 12–2. 10W Power Amplifier Components (Cont'd).

Location	Style	Description	Group
CHOKES			
L01	9646A07H41	220.0 μH	01,02
L04	3532A37H01	3443-58 270 μH .33 OHM 10%	01,02
L05	3532A37H01	3443-58 270 μH .33 OHM 10%	01,02
CONNECTORS			
JU1	9640A47H01	3 POSITION	01
DIODES			
D03	836A928H08	1N4007 1000 V 1 A	01,02
D04	836A928H08	1N4007 1000 V 1 A	01,02
D05	836A928H08	1N4007 1000 V 1 A	01,02
INDUCTORS			
L02	3537A46H34	360 μH	01,02
L03	3537A46H34	360 μH	01,02
LINEAR ICs			
QN1	3533A63H01	MPQ3906 QUAD PNP ARRAY 40 V 0.2 A	01,02
QN2	3533A64H01	MPQ3904 QUAD NPN ARRAY 40 V 0.2 A	01,02
QN3	3533A64H01	MPQ3904 QUAD NPN ARRAY 40 V 0.2 A	01,02
LEDs			
D06	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01,02
POTENTIOMETERS			
R41	3536A55H05	50 K 10%	01,02
R53	3535A32H04	2 K OHM 10%	01,02
R54	3536A55H06	500 OHM 10%	01
RELAYS			
K01	1484B33H01	AROMAT TYPE ST1E-DC 12 V	01
RESISTORS			
R01	RM1241FQB0	1.24 KILOHMS 1% 0.25 W METAL FILM	01,02
R02	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02
R03	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02
R04	RM2741FQB0	2.74 KILOHMS 1% 0.25 W METAL FILM	01,02
R05	RM2741FQB0	2.74 KILOHMS 1% 0.25 W METAL FILM	01,02
R06	RM1101FQB0	1.10 KILOHMS 1% 0.25 W METAL FILM	01,02
R07	RM1101FQB0	1.10 KILOHMS 1% 0.25 W METAL FILM	01,02
R08	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02
R09	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02
R10	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02
R11	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02

Table 12–2. 10W Power Amplifier Components (Cont'd).

Location	Style	Description	Group
RESISTORS (Cont'd)			
R12	RM1101FQB0	1.10 KILOHMS 1% 0.25 W METAL FILM	01,02
R13	RM536AFQB4	53.6 OHMS 1% 0.25 W METAL FILM	01,02
R14	RM1101FQB0	1.10 KILOHMS 1% 0.25 W METAL FILM	01,02
R15	RM536AFQB4	53.6 OHMS 1% 0.25 W METAL FILM	01,02
R16	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02
R17	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02
R18	RM1430FQB1	143 OHMS 1% 0.25 W METAL FILM	01,02
R20	RM6491FQB0	6.49 KILOHMS 1% 0.25 W METAL FILM	01,02
R21	RM1331FQB0	1.33 KILOHMS 1% 0.25 W METAL FILM	01,02
R22	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02
R23	RM1650FQB1	165 OHMS 1% 0.25 W METAL FILM	01,02
R25	RM1400FQB1	140 OHMS 1% 0.25 W METAL FILM	01,02
R26	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02
R27	RM150AFQB4	15.0 OHMS 1% 0.25 W METAL FILM	01,02
R28	RC330AJH59	33 OHMS 5% 0.5 W CARBON COMP	01,02
R29	RC330AJH59	33 OHMS 5% 0.5 W CARBON COMP	01,02
R30	RW330CJ2A5	0.33 OHMS 5% 2 W WIREWOUND	01,02
R31	RW330CJ2A5	0.33 OHMS 5% 2 W WIREWOUND	01,02
R32	RM150AFQB4	15.0 OHMS 1% 0.25 W METAL FILM	01,02
R33	RM210BFQB7	2.10 OHMS 1% 0.25 W METAL FILM	01,02
R34	RC680BJ1E3	6.8 OHMS 5% 1 W CARBON COMP	01,02
R35	RM210BFQB7	2.10 OHMS 1% 0.25 W METAL FILM	01,02
R36	RM210BFQB7	2.10 OHMS 1% 0.25 W METAL FILM	01,02
R37	RM210BFQB7	2.10 OHMS 1% 0.25 W METAL FILM	01,02
R38	RM210BFQB7	2.10 OHMS 1% 0.25 W METAL FILM	01,02
R39	RM210BFQB7	2.10 OHMS 1% 0.25 W METAL FILM	01,02
R40	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R42	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R43	RM4991FQB0	4.99 KILOHMS 1% 0.25 W METAL FILM	01,02
R44	RM2001FQB0	2.00 KILOHMS 1% 0.25 W METAL FILM	01,02
R45	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R46	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R47	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R48	RB3904JQB3	3.9 MEGOHMS 5% 0.25 W CARBON FILM	01,02
R49	RC3601J167	3.6 KILOHMS 5% 1 W CARBON COMP	01,02
R50	RC1501J167	1.5 KILOHMS 5% 1 W CARBON COMP	01
R51	RC680BJ1E3	6.8 OHMS 5% 1 W CARBON COMP	01,02
R52	RB2700JQB2	270 OHMS 5% 0.25 W CARBON FILM	01,02
R55	RM3010FQB1	301 OHMS 1% 0.25 W METAL FILM	01,02

(Continued on next page.)

Table 12–2. 10W Power Amplifier Components (Cont'd).

Location	Style	Description	Group
TIP JACKS			
TJ1	3532A53H09	BLUE	01,02
TJ2	3532A53H03	BLACK PC MOUNT	01,02
TRANSFORMERS			
T01	1495B84G01	1:3.75 OUTPUT	01,02
T02	1498B24G01	1:3 INPUTS	01,02
TRANSISTORS			
Q01	3533A59H01	MPSUO2 40 V 0.8 A 1 W NPN	01,02
Q02	3533A60H01	MPSU52 40 V 1.5 A 1 W PNP	01,02
Q03	3532A45H01	D40D13 75 V 1.0 A 6.2 W NPN	01,02
Q04	3532A45H02	D41D13 75 V 1 A 6.2 W PNP	01,02
Q05	3532A45H01	D40D13 75 V 1.0 A 6.2 W NPN	01,02
Q06	3532A45H19	D44VH10 80 V 15 A 83 W NPN	01,02
Q07	3532A45H20	D45VH10 80 V 15 A 83 W PNP	01,02
Q08	3509A35H09	MPS8599 80 V 0.5 A 0.35 W PNP	01,02
ZENERS			
D01	862A606H06	1N751A 5.1 V 5% 0.4 W	01,02
D02	862A606H06	1N751A 5.1 V 5% 0.4 W	01,02

Chapter 13. RF Interface Module

Schematic	1609C32-8
Parts List	1609C32-8

13.1 RF Interface Module Description

The RF Interface Module, used with the TC–10B/TCF–10B, has several functions:

- Receives RF input from 10W PA Module.
- Matches output impedance at 50, 75, or 100 ohms.
- Low-pass filter covers RF spectrum up to 550 kHz.
- Permits 2- or 4-wire operation.
- Protects against line surges with a gas tube device.

13.1.1 RF Interface Control Panel

(This panel is shown in Figure 1-1.)

Operator controls consist of Test Jacks:

TJ1 Line In

TJ2 Line Common

TJ3 Receiver In

TJ4 Receiver Common

13.1.2 RF Interface PC Board

(The RF Interface PC Board is shown in Figure 13-1.)

Operator controls are as follows:

Matching Impedance Jumpers

JU4 50 ohms

JU3 75 ohms

JU2 100 ohms

2-wire or 4-wire RF Termination

JU1/JU5	"IN"	2-wire
JU1/JU5	"OUT"	4-wire

Attenuator Override Jumper (JU6)

NORM Sensitivity	70 Vrms at 5,000 ohms
HIGH Sensitivity	17 Vrms at 1,000 ohms

13.2 RF Interface Circuit Description

This module receives RF input from the 10W PA Module at pins A16/C16 and A18/C18, and feeds the power through a balanced low-pass filter with a 550 kHz cutoff (L3, L4, L1, L2 and associated components). RF is fed through transformer T1, for matching 50 ohm (JU4), 75 ohm (JU3), or 100 ohm (JU2) resistance to the RF line output (45 Vrms maximum) at pins 12A/12C and 10A/10C, which provide the two-wire UHF (J1) connection on the Rear Panel.

Four-Wire Receiver input is provided at pins 24 A/C and 22 A/C via the 4-wire BNC (J2) connector on the Rear Panel. Jumpers JU1 and JU5 simultaneously connect the four-wire Receiver input to RF line output:

- IN settings for 2-wire operation
- OUT settings for 4-wire operation

Isolation transformer T2, together with series resistor R1, forms an attenuator with 13 dB loss. Receiver input (at pins 28 A/C) is adjusted by jumper JU6:

- When in the NORM position, Receiver maximum input is 70 Vrms at 5,000 ohms
- When in the HIGH position, JU6 overrides the attenuator, providing lower input impedance (Receiver maximum input is 17 Vrms at 1,000 ohms).

13.3 RF Interface Troubleshooting

With the PC Board plugged into the chassis, you can monitor the voltage output to the RF line at TJ1 and TJ2. You can monitor receiver input at TJ3 and TJ4.

Should a fault occur in the RF Interface Module, you can remove the PC board and check the components by conventional means.

13.3.1 Capacitors

Remove from the circuit with jumpers JU2, JU3 and JU4 and check for shorts, dissipation factor, and capacitance. (Perform checks using a signal of 10 kHz or higher.)

13.3.2 Inductors

Check with an ohmmeter.

13.3.3 Transformers

Check for open circuits.

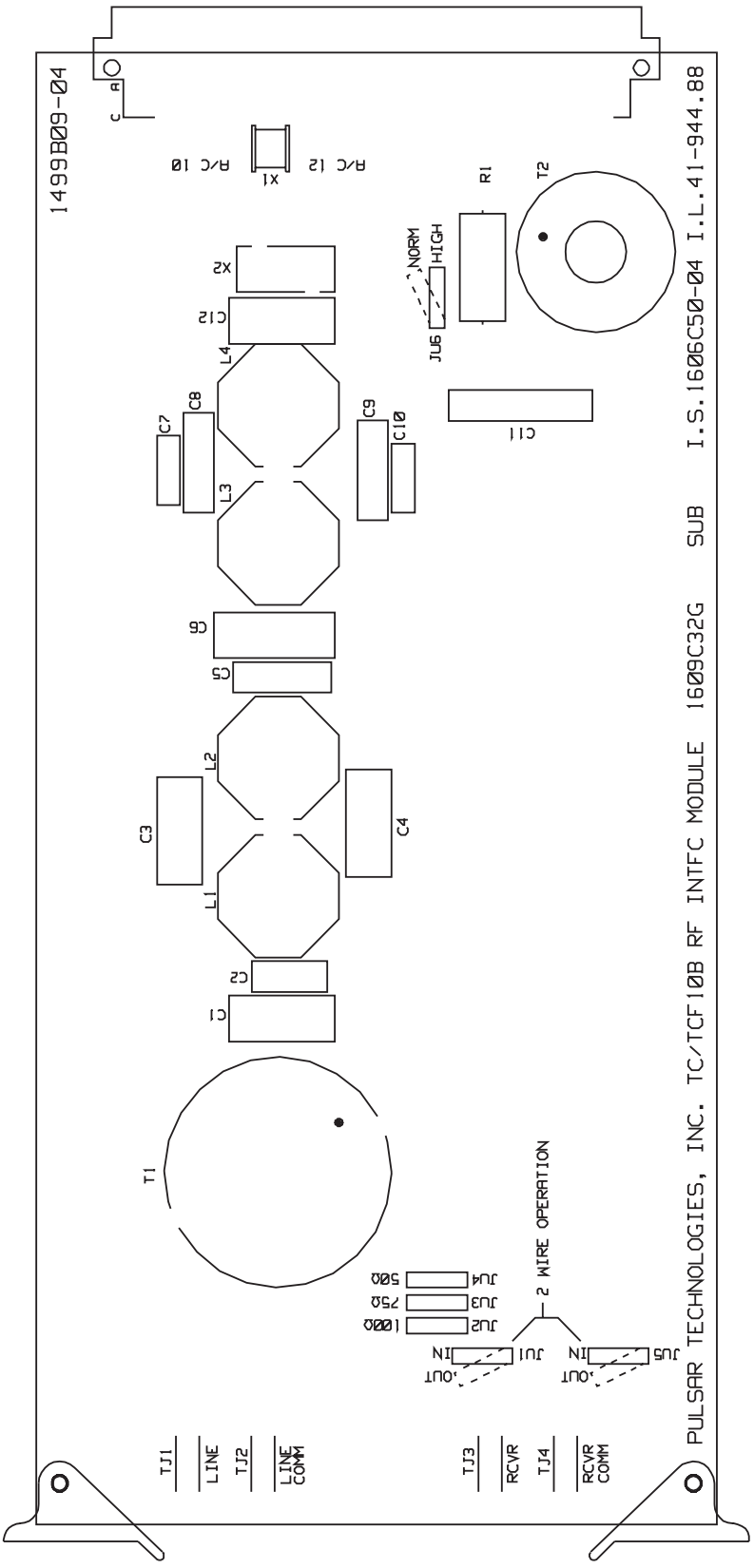

Figure 13–1. TC–10B/TCF–10B RF Interface PC Board (1609C32; Sheet 3 of 3).

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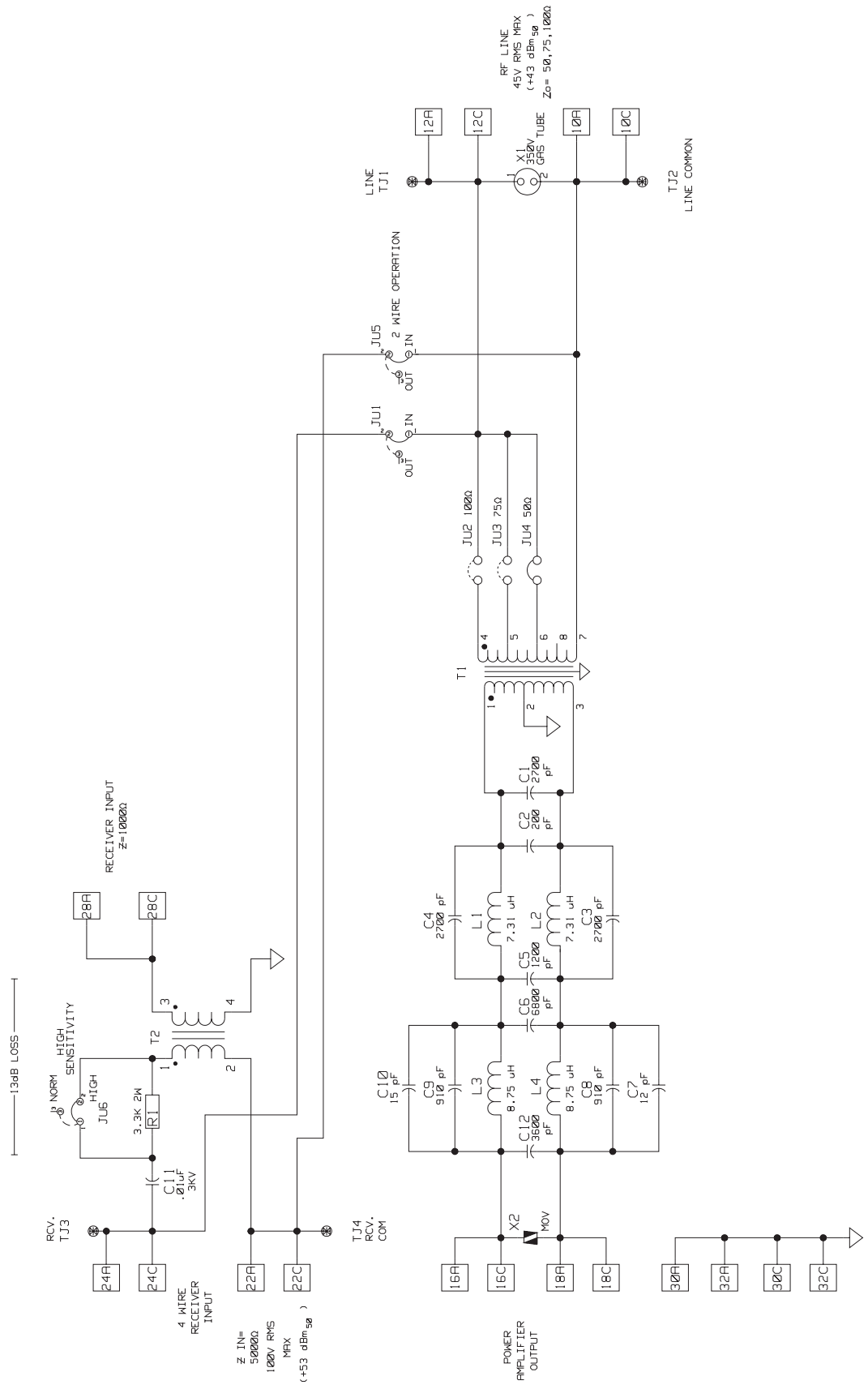


Figure 13–2. TC–10B/TCF–10B RF Interface PC Board (1609C32; Sheet 1 of 3).

Table 13–1. RF Interface Module Components (1609C32).

Location	Style	Description	Group
CAPACITORS			
C1	CR2701GVA6	2700 pF 2% 500 V DIPPED MICA	01
C2	CR2000GV91	200 pF 2% 500 V DIPPED MICA	01
C3	CR2701GVA6	2,700 pF 2% 500 V DIPPED MICA	01
C4	CR2701GVA6	2,700 pF 2% 500 V DIPPED MICA	01
C5	CR1201GVA6	1,200 pF 2% 500 V DIPPED MICA	01
C6	CR6801GV91	6,800 pF 2% 500 V DIPPED MICA	01
C7	CR120AJV67	12 pF 5% 500 V DIPPED MICA	01
C8	CR9100GVA6	910 pF 2% 500 V DIPPED MICA	01
C9	CR9100GVA6	910 pF 2% 500 V DIPPED MICA	01
C10	CR150AJV17	15 pF 5% 500 V DIPPED MICA	01
C11	CQ1002M380	.01 μF 20% 3,000 V Z5U CERAMIC DISC	01
C12	CR3601GVA6	3,600 pF 2% 500 V DIPPED MICA	01
INDUCTORS			
L1	1602C75G09	HYBRID FILTER 7.31 μH	01
L2	1602C75G09	HYBRID FILTER 7.31 μH	01
L3	1602C75G10	HYBRID FILTER 8.75 μH	01
L4	1602C75G10	HYBRID FILTER 8.75 μH	01
JUMPERS			
JU1	3532A54H02	PLUG IN	01
JU2	3532A54H02	PLUG IN	01
JU3	3532A54H02	PLUG IN	01
JU4	3532A54H02	PLUG IN	01
JU5	3532A54H02	PLUG IN	01
JU6	3532A54H02	PLUG IN	01
RESISTORS			
R1	RC3901J249	3.3 KILOHMS 5% 2 W CARBON COMP	01
SURGE PROTECTORS			
X1	3532A90H01	350 V GASTUBE TO8-350B	01
TIP JACKS			
TJ1	3532A53H03	BLACK PC MOUNT	01
TJ2	3532A53H03	BLACK PC MOUNT	01
TJ3	3532A53H03	BLACK PC MOUNT	01
TJ4	3532A53H03	BLACK PC MOUNT	01
TRANSFORMERS			
T1	1493B54G01	RECEIVE	01
T2	714B677G02	1:1 10 K INTERSTAGE	01
VARISTORS			
X2	3509A31H09	V68ZA10	01

USER NOTES

Chapter 14. Receiver Module & Synthesizer Module

Schematic	1606C32-21
Parts List	1606C32-21

Table 14–1. 1606C32 Styles and Descriptions.

Group	TCF-10B	TC-10B
G01 (1,200 Hz)	Extra Wide Band	Wide Band
G02 (600 Hz)	Medium/ Wide Band	Narrow Band
G03 (300 Hz)	Narrow Band	—

14.1 Receiver Module Description

The TC–10B/TCF–10B Receiver Module passes the RF signal (from the RF Interface Module) through a low-pass filter and attenuator to the first mixer, whose injection is supplied by the frequency synthesizer. The output of the first mixer, at 5.02 MHz, is fed through the first amplifier to a crystal bandpass filter that provides most of the receiver selectivity. The IF signal, after passing through the second and third amplifiers, is mixed (at the second mixer) with the 5 MHz reference from the crystal oscillator, is filtered (bandpass filter) and buffered, providing a 20 kHz output.

The TC–10B has two Receiver bands; the TCF–10B has three Receiver bands for a variety of applications, as shown in Table 14-1 (see the Schematic, Figure 14-3 and Figure 14-4, and Parts List for further detail).

14.1.1 Receiver Control Panel

(This panel is shown in Figure 1-1.)

Operator controls are as follows:

Thumbwheel switches

The Receiver Control Panel's thumbwheel switches have indicator windows showing a frequency range.

Potentiometer

The potentiometer (R3), LEVEL ADJUST attenuator adjusts receiver input (receiver margin sensitivity).

Test Jacks

TJ2 RCV blue

TJ1 INPUT yellow

TJ3 COM green

14.1.2 Receiver PC Board

(The Receiver PC Board is shown in Figure 14-2.)

Operator controls are as follows:

Jumper: JU1 - Disable/Norm

"Disable" allows the Receiver to be turned "OFF" when the Transmitter is keyed. "Norm" has no effect. This jumper is no longer used.

⚠ CAUTION

SOME TC–10B USERS HAVE INADVERTENTLY PLACED JU1 (ON THE RECEIVER MODULE) IN THE "DISABLE" POSITION, WHEN IT SHOULD HAVE BEEN IN "NORMAL." IF THE RELAY YOU ARE USING WITH THE TC–10B REQUIRES A RECEIVER OUTPUT DURING TRANSMIT, JU1 MUST BE IN "NORMAL."

Variable Capacitors

C19 Tunes the first mixer injection filter.

C68 Sets the crystal oscillator to 5 MHz

Potentiometers

R67 Voice IF adjustment

R68 IF Gain Control

Test Points

TP1 5 MHz oscillator Reference

TP2 Injection Voltage

TP3 Injection Voltage

TP4 5.02 IF Output from 2nd Mixer

TP5 20 kHz Output

14.2 Receiver Circuit Description

The Receiver Module (see Figure 14-3 and Figure 14-4, Schematic 1606C32S) passes the RF signal (from the RF Interface Module) through a low-pass filter and attenuator to the first mixer, whose injection is supplied by the frequency synthesizer. The output of the first mixer, at 5.02 MHz, is fed through the first amplifier to a crystal bandpass filter that provides most of the receiver selectivity. The IF signal, after passing through the second and third amplifiers, is mixed (at the second mixer) with the 5 MHz reference from the crystal oscillator, is filtered (bandpass filter) and buffered, providing a 20 kHz output.

The RF input of 30 to 535 kHz is fed to connector pin C-28 with the return or common pins A/C-30 and 32. TJ1 and TJ2 are on the front panel for ease in measuring line input and receiver input levels. Zener diodes D1 and D2 provide overload protection for the receiver input circuit. Jumper JU1 allows the receiver to be disabled when transmitting, if desired.

The RF input is fed through a front panel level adjust attenuator (R3) and through a low pass filter to the mixer (I_3). The combination of R4, R5 and R6 provides an attenuator and serves to maintain a 50 ohm termination at the input of the low pass filter (L1, L2, C1, C2 and C3). This attenuator has a 7 dB loss. The attenuator formed by R7, R8 and R9 provides the proper termination for I_3 and also has a 7 dB loss. The low pass filter has a cut-off frequency of 600 kHz.

The synthesizer supplies the second input to the mixer (I_3); this input is always 5.02 MHz plus the channel frequency. (Selection of the receiver channel is done by the front panel thumbwheel switches.) The mixer injection voltage is supplied by the synthesizer to I_1 and I_2 and associated components. I_1 and I_2 are high frequency, low impedance drivers. A low pass filter (L8, L9, L10, L11, C18 and C19) removes harmonics of the injection frequency. R13 through R17 form a matching network for low pass filter termination and mixer matching.

The first mixer (I_3) is a high level type that can withstand large input levels without creating intermodulation products. The oscillator level, injected at pins 7 and 8 of the mixer, is +17 dBm (1.6 Vrms). The 5.02 MHz mixer output, on pins 1 and 2, is fed through a diplexer to the first IF Amplifier (Q1/Q2 and associated components). The diplexer provides 50 ohm termination to all frequencies, but only passes frequencies below 6 MHz. The first IF Amplifier is a high level, low distortion amplifier capable of delivering 100 milliwatts maximum into R24. The amplifier has approximately 14 dB of power gain. A matching attenuator network (R69, R70 and R71) establishes the proper driving impedance for filter FL1. This network has 6 dB loss.

Filter FL1 determines the bandwidth of the receiver. Extra Wide Band (approximately 1.2 kHz), Wide Band (approximately 600 Hz) and Narrow Band (approximately 300 Hz) are available. The stop band attenuation of the filter is greater than 60 dB. FL1 has about 3.5 dB loss. The output of the filter is fed to the 2nd IF amplifier (see Schematic sheet 2, Figure 14-4). A second path from the 1st IF Amplifier is fed to Q3 and Q4 and associated components, which form a buffer amplifier to provide an auxiliary output for the optional voice adapter. This output is brought to connector pins A/C-24. R67 is an adjustment for setting the voice output level.

The combination of I_4, I_5, T2 and associated components form the 5.02 MHz IF amplifier (sheet 2). Amplifier I_5 is resonated by L15 and C42; R68 adjusts the overall gain of the I_4-I_5 combination to present the proper level to the second mixer (I_6). I_4 and I_5 have a combined voltage gain of approximately 54 to 84 dB, depending on the setting of R68. Transformer (T2) has a 16 to 1 impedance ratio and matches the 50 ohm mixer input (pins 1 and 7) to the 800 ohm output of I_5 and R40. There is a voltage loss of 18 dB from I5 pins 7 and 8 to the input of the mixer.

The second mixer (I_6) has a 5.02 MHz input from the IF amplifier and a 5 MHz input from the crystal oscillator. The output from the second mixer, 20 kHz, is fed through a bandpass filter to the output on pin A-28. This mixer has a 5 MHz injection of +7 dBm (.5 Vrms) applied to I_6 pins 2 and 8. The 5.0 MHz reference crystal oscillator is adjusted to 5 MHz by C68, and consists of QN1 (A, B, C and D). Because the input is 5.02 MHz and the injection frequency is 5.00 MHz, the mixer output is 20.0 kHz plus other mixer products. An active bandpass filter is configured from the combination of I_7 and associated components. It is used to drive the receiver output, at connector pin A-28. This filter is tuned to a center frequency of 20 kHz with approximately 4 kHz bandwidth. The bandpass filter has 32 dB voltage gain.

On-board voltage regulation and reverse voltage protection is provided by D3, D4, D5, D6 and associated components. All functional circuit blocks operate from +18.6 and +3.6 or -18.6 and -3.6 to provide +15 Vdc for operation. The synthesizer uses both plus and minus 18.6 and 3.6. The synthesizer plugs onto the PC Board with J1, J2 and J3. You may remove it by unscrewing the three hold down screws and unplugging it.

RF filtering is provided by L6, L7, L12, L13, L18 and L19 (Sheet 1) and by R28, R30, R31 and R34 (Sheet 2) to prevent stray coupling from circuit to circuit. All RF bypassing is to common.

14.3 Receiver Troubleshooting

With the PC Board plugged into the chassis, you can check the following functions:

14.3.1 Input Signal

You can use the following three test points on the control panel to indicate if a signal is getting to the module:

TJ1	Line Input
TJ2	Mixer Input
TJ3	Common

Monitor between TJ1 and TJ3 with a selective Level voltmeter (or equivalent)

Proper input must be:

- (G01) 1,200 Hz bandwidth (> 15 mV rms)

- (G02) 600 Hz bandwidth, > 5 mV rms
- (G03) 300 Hz bandwidth, > 5 mV rms

For normal operation, this input signal should be ∅ 15 dB above the threshold level.

Monitor between TJ1 and TJ2

Proper input should be:

- (G01) 1,200 Hz bandwidth (72 μV rms)
- (G02) 600 Hz bandwidth (24 mV rms)
- (G03) 300 Hz bandwidth (24 mV rms)

You may adjust this level with the Level Adjust Attenuator (R3).

14.3.2 Output Signal

You can check the output signal (20 kHz) at TP5 or pin A-28. When the input threshold voltage is set per the paragraph "Monitor between TJ1 and TJ3 with a selective Level voltmeter (or equivalent)" above, The 20 kHz output should be 63 mV rms. If there is no voltage output at 20 kHz, you can perform the tests described below.

> NOTE
>
> If the foregoing levels are correct, but the Receiver does not function, place the Receiver Module on an extender board.

Synthesizer

The 5 MHz crystal oscillator level should be 560 mV rms at pin 12 of the PC Board connector (J1).

Injection

The injection voltage between TP2 and TP3 should be 3.5 Vp-p; the injection frequency should be 5.02 MHz plus the channel frequency. This differential input is measured from TP2 to TJ3 (common) and from TP3 to TJ3 (common). If the injection voltage is low or non-existent, you can remove the Synthesizer to determine if the problem is in the Synthesizer or I_1 and/or I_2.

When removing the Synthesizer, you must be careful to keep the hold-down screws captive. Unscrew the three Synthesizer hold-down screws partially and partially unplug the Synthesizer. Continue this procedure until the Synthesizer is completely unplugged. Do not remove any of the screws completely (about 8 turns should be enough).

You may apply a 5.02 MHz plus the channel frequency signal between Synthesizer connector (J3) pins 2 and 3 to check the operation of I_1, I_2, and the injection filter. Use the variable capacitor (C19) to adjust for maximum output at TP2/TP3.

The 5.02 MHz plus the channel frequency signal should consist of the following:

- Two 5 Vp-p square wave signals, 180 degrees out-of-phase (reference to ground),

or• With the additional circuitry, as shown in Figure 14-1, one 10 Vp-p square wave signal may be used.

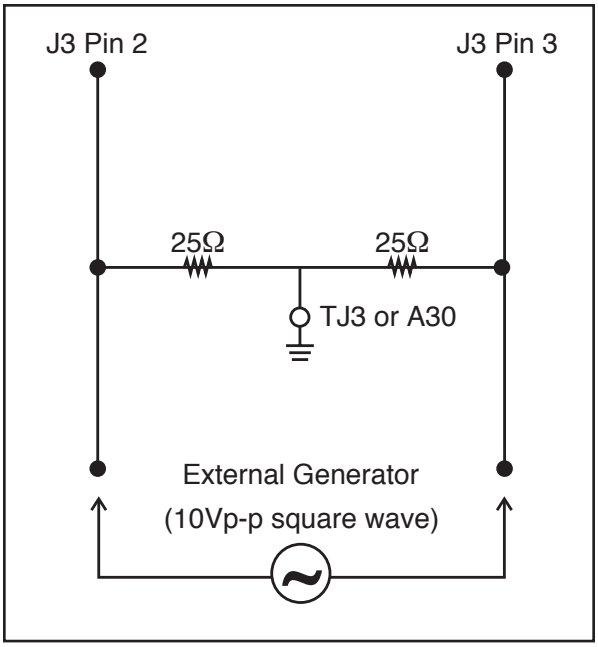


Figure 14–1. Additional Circuitry at Test Jack (TJ3).

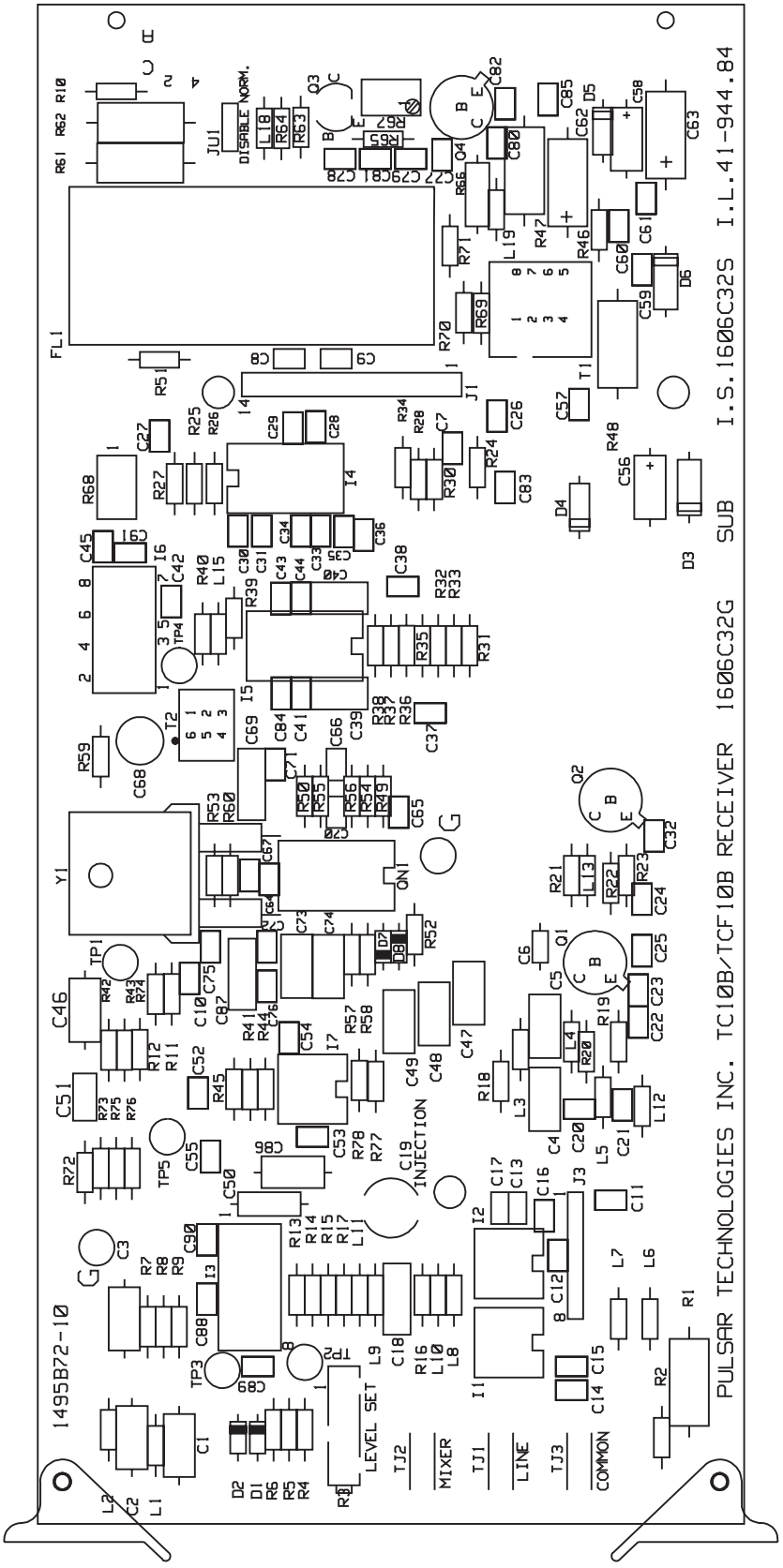


Figure 14–2. TC–10B/TCF–10B Receiver PC Board (1495B72; Sheet 8 of 8).

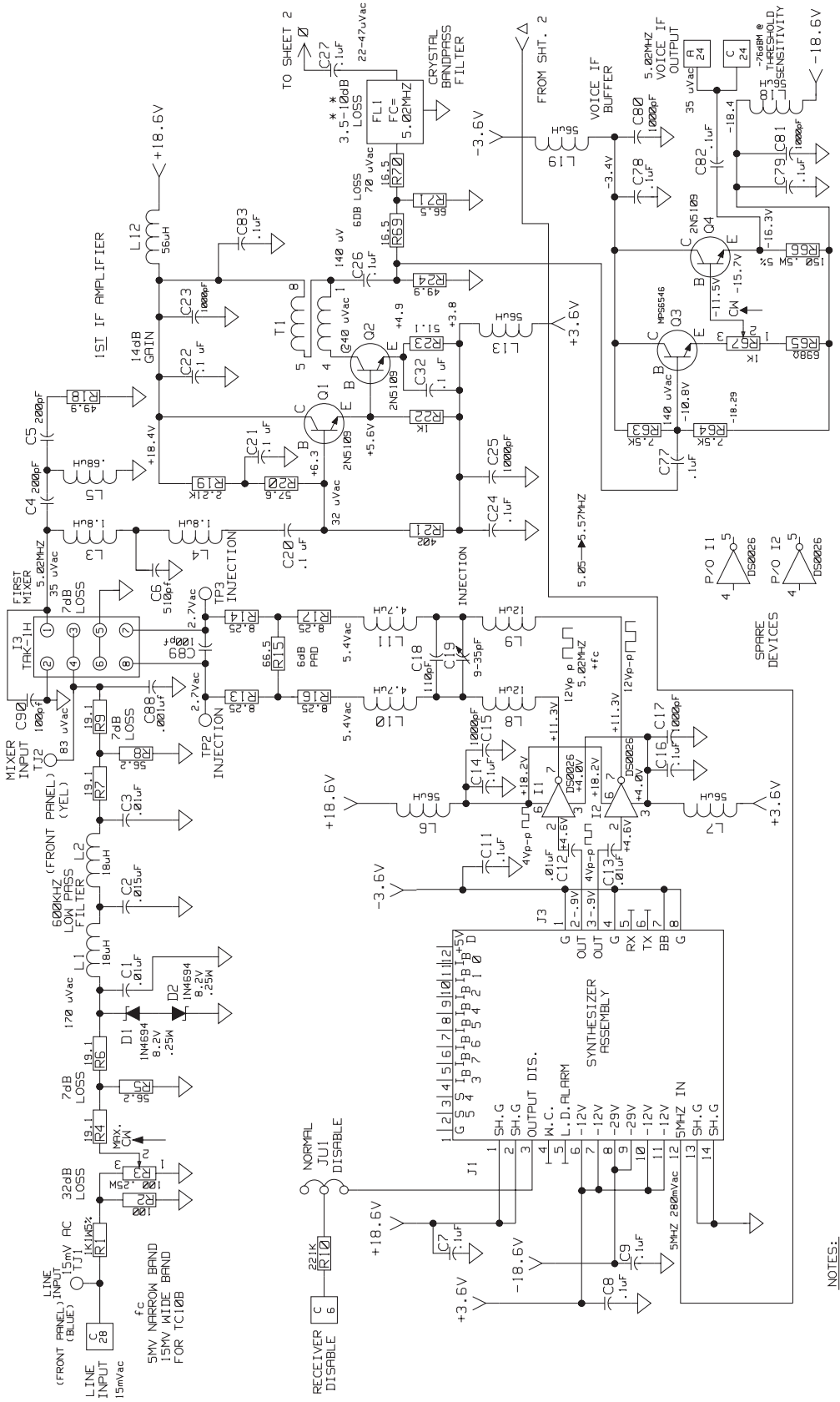


Figure 14–3. TC–10B/TCF–10B Receiver Schematic (1606C32; Sheet 4 of 5).

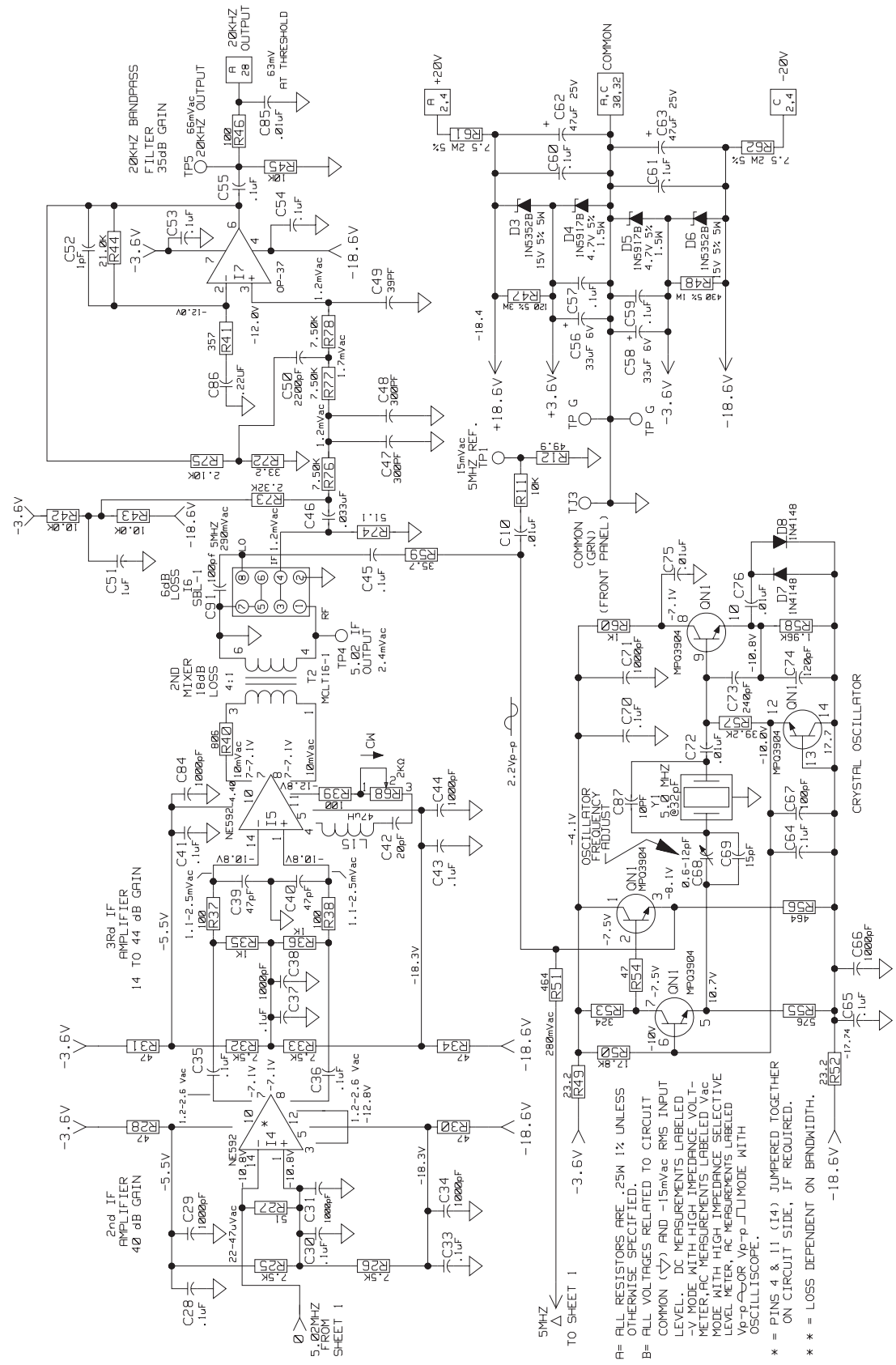
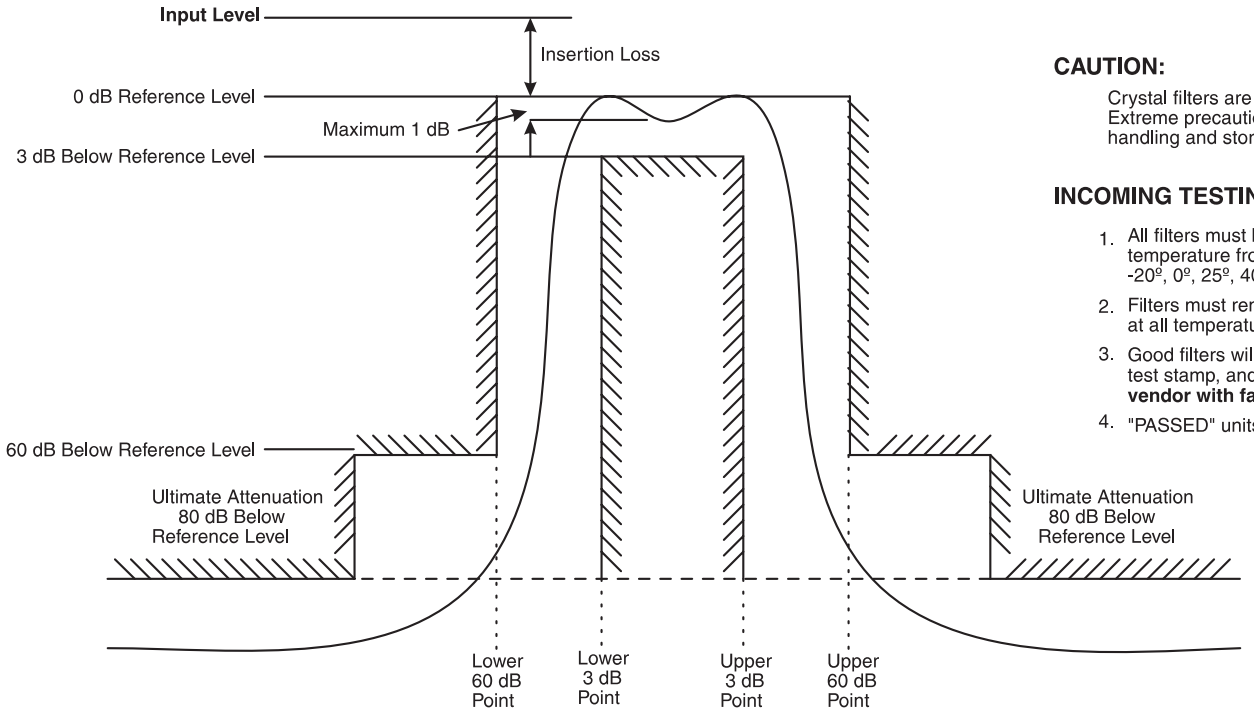


Figure 14–4. TC–10B/TCF–10B Receiver Schematic (1606C32; Sheet 5 of 5).



CAUTION:

Crystal filters are very fragile.
Extreme precautions must be taken during handling and storage to prevent damage.

INCOMING TESTING REQUIREMENTS:

1. All filters must be measured over temperature from -20º C to +60º C using -20º, 0º, 25º, 40º, and 60º C.
2. Filters must remain within their specifications at all temperatures.
3. Good filters will be marked with a "PASSED" test stamp, and **reject units returned to vendor with failure data.**
4. "PASSED" units will then be placed in stock.

STYLE NO. 1353D78H01 NARROW BAND TCF-10B (3 dB BW 300 Hz)

5.02 MHz CRYSTAL BANDPASS FILTER

1. ELECTRICAL SPECIFICATIONS: (See Section 14.3.1). Note that peak response is used for 0dB reference.

1.1 Upper 3 dB point 5.020110 MHz minimum. Lower 3 dB point 5.019890 MHz maximum.

1.2 Lower 60 dB point 5.019500 MHz minimum. Upper 60 dB point 5.020500 MHz maximum.

1.3 Ultimate attenuation [3] 80 dB outside frequency range of 5.02 MHz ±10 kHz.

1.4 Passband ripple 1.0 dB peak-to-valley maximum.

1.5 Insertion loss 14.0 dB maximum.

1.6 Terminations 50 ohms resistive input and output.

2.0 ENVIRONMENTAL SPECIFICATIONS

2.1 Operating temperature: The above electrical specifications shall apply over the temperature range -20°C to +70°C.

2.2 Storage temperature: -30°C to +85°C.

2.3 Shock: 30 G 11 ms.

2.4 Vibration: Standard commercial low frequency 0–60 Hz .06 IN displacement.

STYLE NO. 1353D78H02 WIDEBAND/MEDIUM BAND TCF–10B/ NARROW BAND TC-10B (3 dB BW 600 Hz)

5.02 MHz CRYSTAL BANDPASS FILTER

1. ELECTRICAL SPECIFICATIONS: (See Section 14.3.1) Note that peak response is used for 0 dB reference.

1.1 Upper 3 dB point 5.020260 MHz minimum. Lower 3 dB point 5.019740 MHz maximum.

1.2 Lower 60 dB point 5.019000 MHz minimum. Upper 60 dB point 5.021000 MHz maximum.

1.3 Ultimate attenuation [3] 80 dB outside frequency range of 5.02 MHz ±20 kHz.

1.4 Passband ripple 1.0 dB peak-to-valley maximum.

1.5 Insertion loss 7.0 dB maximum.

1.6 Terminations 50 ohms resistive input and output.

2.0 ENVIRONMENTAL SPECIFICATIONS

2.1 Operating temperature: The above electrical specifications shall apply over the temperature range -20°C to +70°C.

2.2 Storage temperature: -30°C to +85°C.

2.3 Shock: 30 G 11 ms.

2.4 Vibration: Standard commercial low frequency 0–60 Hz .06 IN displacement.

STYLE NO. 1353D78H03 EXTRA WIDEBAND TCF-10B/ WIDEBAND TC–10B (3 dB BW 1,200 Hz)

5.02 MHz CRYSTAL BANDPASS FILTER

1. ELECTRICAL SPECIFICATIONS: (See Section 14.3.1). Note that peak response is used for 0 dB reference.

1.1 Upper 3 dB point 5.020510 MHz minimum. Lower 3 dB point 5.019490 MHz maximum.

1.2 Lower 60 dB point 5.018000 MHz minimum. Upper 60 dB point 5.022000 MHz maximum.

1.3 Ultimate attenuation [3] 80 dB outside frequency range of 5.02 MHz ±40 kHz.

1.4 Passband ripple 1.0 dB peak-to-valley maximum.

1.5 Insertion loss 5.0 dB maximum.

1.6 Terminations 50 ohms resistive input and output.

2.0 ENVIRONMENTAL SPECIFICATIONS

2.1 Operating temperature: The above electrical specification shall apply ove the temperature range -20°C to +70°C.

2.2 Storage temperature: -30°C to +85°C.

2.3 Shock: 30 G 11 ms.

2.4 Vibration: Standard commercial low frequency 0–60 Hz .06 IN displacement.

Figure 14–5. Crystal Filter Characteristics (1353D78; Sheet 2 of 2).

Table 14–2. Receiver Module Components (1606C32).

Location	Style	Description	Group
CAPACITORS			
C01	CF1002JP78	0.01 μF 5% 200 V MET POLYCARB	01,02,03
C02	CF1502GP78	0.015 μF 2% 200 V MET POLYCARB	01,02,03
C03	CF1002JP78	0.01 μF 5% 200 V MET POLYCARB	01,02,03
C04	CR2000JVE0	200 pF 5% 500 V DIPPED MICA	01,02,03
C05	CR2000JVE0	200 pF 5% 500 V DIPPED MICA	01,02,03
C06	CR5100GV67	510 pF 2% 500 V DIPPED MICA	01,02,03
C07	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C08	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C09	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C10	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C11	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C12	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C13	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C14	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C15	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C16	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C17	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C18	CR1100JV67	110 pF 5% 500 V DIPPED MICA	01,02,03
C20	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C21	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C22	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C23	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C24	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C25	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C26	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C27	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C28	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C29	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C30	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C31	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C33	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C34	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C35	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C36	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C37	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C38	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C39	CR470AJV67	47 pF 5% 500 V DIPPED MICA	01,02,03
C40	CR470AJV67	47 pF 5% 500 V DIPPED MICA	01,02,03
C41	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C42	CR200AJR67	20 pF 5% 300 V DIPPED MICA	01,02,03
C43	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C44	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C45	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01,02,03
C46	CF3302JL78	0.033 μF 5% 100 V MET POLYCARB	01,02,03
CAPACITORS (Cont'd)			
C47	CR3300JLE0	330 pF 5% 100 V DIPPED MICA	01,02,03

Table 14–2. Receiver Module Components (Cont'd).

Location	Style	Description	Group
C48	CR3000JRE0	300 pF 5% 300 V DIPPED MICA	01,02,03
C49	CR390AJVE0	39 pF 5% 500 V DIPPED MICA	01,02,03
C50	CF2201GU70	2200 pF 2% 400 V MET POLYCARB	01,02,03
C51	CP1004MH54	1.0 µF 20% 50 V MONO CERAMIC	01,02,03
C52	CR100BDR67	1 pF +/-0.5 pF 300 V DIPPED MICA	01,02,03
C53	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C54	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C55	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C56	CJ3305MA72	33 µF 20% 6 V MOLDED TANTALUM	01,02,03
C57	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C58	CJ3305MA72	33 µF 20% 6 V MOLDED TANTALUM	01,02,03
C59	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C60	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C61	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C62	CJ4705ME72	47 µF 20% 25 V MOLDED TANTALUM	01,02,03
C63	CJ4705ME72	47 µF 20% 25 V MOLDED TANTALUM	01,02,03
C64	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C65	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C66	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C67	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	01,02,03
C68	863A539H02	0.6-12 pF 50 PPM TRIMMER	01,02,03
C69	CR150AJV17	15 pF 5% 500 V DIPPED MICA	01
C70	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C71	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C72	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C73	CR2400JVE0	240 pF 5% 500 V DIPPED MICA	01,02,03
C74	CR1200JVE0	120 pF 5% 500 V DIPPED MICA	01,02,03
C75	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C76	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C77	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C78	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C79	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C80	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C81	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C82	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C83	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C84	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C85	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	01,02,03
C86	CF2203JL78	0.22 µF 5% 100 V MET POLYCARB	01,02,03
C87	CR100AGV92	10 pF 2% 500 V DIPPED MICA	01,02,03
C88	CP1001KL65	1,000 pF 10% 100 V X7R MONO CERAMIC	01,02,03
C89	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	01,02,03
C90	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	01,02,03
C91	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	01,02,03
CHOKES			
L01	9646A07H28	18.0 µH	01,02,03
L02	9646A07H28	18.0 µH	01,02,03
L03	9646A07H16	1.80 µH	01,02,03

Table 14–2. Receiver Module Components (Cont'd).

Location	Style	Description	Group
L04	9646A07H16	1.80 µH	01,02,03
L05	9646A07H11	.68 µH	01,02,03
L06	9646A07H34	56.0 µH	01,02,03
L07	9646A07H34	56.0 µH	01,02,03
L08	9646A07H26	12.0 µH	01,02,03
L09	9646A07H26	12.0 µH	01,02,03
L10	9646A07H21	4.70 µH	01,02,03
L11	9646A07H21	4.70 µH	01,02,03
L12	9646A07H34	56.0 µH	01,02,03
L13	9646A07H34	56.0 µH	01,02,03
L15	9646A07H33	47.0 µH	01,02,03
L18	9646A07H34	56.0 µH	01,02,03
L19	9646A07H34	56.0 µH	01,02,03
CONNECTORS			
J01	3529A12H11	14 PIN SINGLE ROW HEADER	01,02,03
J03	3529A12H09	8 PIN SINGLE ROW HEADER	01,02,03
CRYSTALS			
Y01	1608C06H01	5.0 MHz (32 pF) CRYSTALS	01,02
Y01	1608C06H03	5.0 MHz (32 pF) CRYSTALS	03
DIODES			
D07	836A928H06	1N4148 75 V 0.01 A	01,02,03
D08	836A928H06	1N4148 75 V 0.01 A	01,02,03
FILTERS			
FL1	1353D78H03	XTAL FILTER 5.02 MHz BW 1,200 Hz	01
FL01	1353D78H01	XTAL FILTER 5.02 MHz BW 300 Hz	03
FL01	1353D78H02	XTAL FILTER 5.02 MHz BW 600 Hz	02
JUMPERS			
JU01	3532A54H01	BLUE CLIP JUMPER	01,02,03
LINEAR ICs			
I5	9646A35H01	NE592N WIDEBAND VIDEO AMP	01,02,03
I01	9646A36H01	DS0026 2-PH MOS CLOCK-DRIVER	01,02,03
I02	9646A36H01	DS0026 2-PH MOS CLOCK-DRIVER	01,02,03
I04	9646A35H01	NE592N WIDEBAND VIDEO AMP	01,02,03
I07	3534A38H01	OP37GZ SINGLE OP-AMP (LO NOISE)	01,02,03
QN01	3533A64H01	MPQ3904 QUAD NPN ARRAY 40 V 0.2 A	01,02,03
MIXERS			
I03	3529A13H03	TAK-1H	01,02,03
I06	3529A13H01	DOUBLE BALANCED SBL-1 I2	01,02,03
POTENTIOMETERS			
R03	3535A32H03	100-OHM 10%	01,02,03
R67	3534A25H04	1 K 25T TOP ADJ.	01,02,03
R68	3534A25H05	2 K-OHM TOP ADJ. VAR.	01,02,03

Table 14–2. Receiver Module Components (Cont'd).

Location	Style	Description	Group
RESISTORS			
R5	RM562AFQB4	56.2 OHMS 1% 0.25 W METAL FILM	01
R8	RM562AFQB4	56.2 OHMS 1% 0.25 W METAL FILM	01
R01	RC1001J167	1.0 KILOHMS 5% 1 W CARBON COMP	01,02,03
R02	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01,02,03
R04	RM191AFQB4	19.1 OHMS 1% 0.25 W METAL FILM	01,02,03
R05	RM562AFQB4	56.2 OHMS 1% 0.25 W METAL FILM	02,03
R06	RM191AFQB4	19.1 OHMS 1% 0.25 W METAL FILM	01,02,03
R07	RM191AFQB4	19.1 OHMS 1% 0.25 W METAL FILM	01,02,03
R08	RM562AFQB4	56.2 OHMS 1% 0.25 W METAL FILM	02,03
R09	RM191AFQB4	19.1 OHMS 1% 0.25 W METAL FILM	01,02,03
R10	RM2213FQ98	221 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R11	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R12	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02,03
R13	RM825BFQB7	8.25 OHMS 1% 0.25 W METAL FILM	01,02,03
R14	RM825BFQB7	8.25 OHMS 1% 0.25 W METAL FILM	01,02,03
R15	RM665AFQB4	66.5 OHMS 1% 0.25 W METAL FILM	01,02,03
R16	RM825BFQB7	8.25 OHMS 1% 0.25 W METAL FILM	01,02,03
R17	RM825BFQB7	8.25 OHMS 1% 0.25 W METAL FILM	01,02,03
R18	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02,03
R19	RM2211FQB0	2.21 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R20	RM576AFQB4	57.6 OHMS 1% 0.25 W METAL FILM	01,02,03
R21	RM4020FQB1	402 OHMS 1% 0.25 W METAL FILM	01,02,03
R22	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R23	RM100AFQB4	10.0 OHMS 1% 0.25 W METAL FILM	01,02,03
R24	RM499AFQB4	49.9 OHMS 1% 0.25 W METAL FILM	01,02,03
R25	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R26	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R27	RM511AFQB4	51.1 OHMS 1% 0.25 W METAL FILM	01,02,03
R28	RB470AJQB2	47 OHMS 5% 0.25 W CARBON FILM	01,02,03
R30	RB470AJQB2	47 OHMS 5% 0.25 W CARBON FILM	01,02,03
R31	RB470AJQB2	47 OHMS 5% 0.25 W CARBON FILM	01,02,03
R32	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R33	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R34	RB470AJQB2	47 OHMS 5% 0.25 W CARBON FILM	01,02,03
R35	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	01,02,03
RESISTORS (Cont'd)			
R36	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R37	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01,02,03
R38	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01,02,03
R39	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01,02,03
R40	RM8060FQB1	806 OHMS 1% 0.25 W METAL FILM	01,02,03
R41	RM3570FQB1	357 OHMS 1% 0.25 W METAL FILM	01,02,03
R42	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R43	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R44	RM2102FQA9	21.0 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R45	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02,03

Table 14–2. Receiver Module Components (Cont'd).

Location	Style	Description	Group
R46	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01,02,03
R47	RC4300J167	430 OHMS 5% 1 W CARBON COMP	01,02,03
R48	RC6800J167	680 OHMS 5% 1 W CARBON COMP	01,02,03
R49	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02,03
R50	RM1782FQA9	17.8 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R51	RM4640FQB1	464 OHMS 1% 0.25 W METAL FILM	01,02,03
R52	RM232AFQB4	23.2 OHMS 1% 0.25 W METAL FILM	01,02,03
R53	RM3240FQB1	324 OHMS 1% 0.25 W METAL FILM	01,02,03
R54	RB470AJQB2	47 OHMS 5% 0.25 W CARBON FILM	01,02,03
R55	RM5760FQB1	576 OHMS 1% 0.25 W METAL FILM	01,02,03
R56	RM4640FQB1	464 OHMS 1% 0.25 W METAL FILM	01,02,03
R57	RM3922FQA9	39.2 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R58	RM1961FQB0	1.96 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R59	RM357AFQB4	35.7 OHMS 1% 0.25 W METAL FILM	01,02,03
R60	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R61	RC750BJ1E3	7.5 OHMS 5% 1 W CARBON COMP	01,02,03
R62	RC750BJ1E3	7.5 OHMS 5% 1 W CARBON COMP	01,02,03
R63	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R64	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R65	RM6980FQB1	698 OHMS 1% 0.25 W METAL FILM	01,02,03
R66	RB1500JHL8	150 OHMS 5% 0.5 W CARBON FILM	01,02,03
R69	RM165AFQB4	16.5 OHMS 1% 0.25 W METAL FILM	01,02,03
R70	RM165AFQB4	16.5 OHMS 1% 0.25 W METAL FILM	01,02,03
R71	RM665AFQB4	66.5 OHMS 1% 0.25 W METAL FILM	01,02,03
R72	RM332AFQB4	33.2 OHMS 1% 0.25 W METAL FILM	01,02,03
R73	RM2321FQB0	2.32 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R74	RM511AFQB4	51.1 OHMS 1% 0.25 W METAL FILM	01,02,03
R75	RM2101FQB0	2.10 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R76	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R77	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
R78	RM7501FQB0	7.50 KILOHMS 1% 0.25 W METAL FILM	01,02,03
TEST POINTS			
TJ01	3532A53H09	BLUE	01,02,03
TJ02	3532A53H07	YELLOW	01,02,03
TJ03	3532A53H08	GREEN	01,02,03
TRANSFORMERS			
T01	1495B82G01	TRANSFORMER	01,02,03
T02	3537A43H01	WIDE BAND TRANSFORMER	01,02,03
TRANSISTORS			
Q4	3493A90H08	2N5109 20 V 0.44 A 2.5 W NPN	01
Q01	3493A90H08	2N5109 20 V 0.44 A 2.5 W NPN	01,02,03
Q02	3532A45H18	MRF476 18 V 1 A 10 W NPN	01,02,03
Q03	3509A35H08	MPS6546 25 V 0.05 A 0.35 W NPN	01,02,03
Q04	3493A90H08	2N5109 20 V 0.44 A 2.5 W NPN	02,03
TRIMMERS			
C19	879A834H03	9.0-35.0 pF TRIMMER	01,02,03

Table 14–2. Receiver Module Components (Cont'd).

Location	Style	Description	Group
ZENERS			
D2	837A693H20	1N4694 8.2 V 5% 0.25 W	01
D5	3535A58H05	1N5917B 4.7 V 5% 1.5 W	01
D01	837A693H20	1N4694 8.2 V 5% 0.25 W	01,02,03
D02	837A693H20	1N4694 8.2 V 5% 0.25 W	02,03
D03	862A288H04	1N5352B 15 V 5% 5 W	01,02,03
D04	3535A58H05	1N5917B 4.7 V 5% 1.5 W	01,02,03
D05	3535A58H05	1N5917B 4.7 V 5% 1.5 W	02,03
D06	862A288H04	1N5352B 15 V 5% 5 W	01,02,03

14.4 Synthesizer Module Description

Schematic	1585C56-20
Parts List	1585C56-20

The Synthesizer Module (1585C56G02), for the TC–10B and TCF–10B, is used to derive the injection frequencies from the 5 MHz crystal oscillator reference for the Receiver Module. The voltage-controlled oscillator (VCO), operating in the range of 90 to 114 MHz, is divided by 20 to produce the local oscillator output of 4.5 to 5.7 MHz. The 5 MHz reference is divided by 500 to produce a 20 kHz reference for the phase detector that generates the dc voltage to control the VCO.

14.4.1 Synthesizer Control Panel

The Synthesizer does not have a control panel of its own; its frequencies are displayed through the Receiver control panel.

14.4.2 Synthesizer PC Board

The Synthesizer PC Board does not contain operator controls.

14.5 Synthesizer Circuit Description

The Synthesizer Module (Schematic 1585C56: Figure 14-6, Figure 14-7, and Figure 1-8) is used to derive the injection frequencies from the 5 MHz crystal oscillator reference for the Receiver Module.

The voltage-controlled oscillator (VCO), operating in the range of 90 to 114 MHz, is divided by 20 to produce the local oscillator output of 4.5 to 5.7 MHz. The 5 MHz reference is divided by 500 to produce a 10 kHz reference for the phase detector that generates the dc voltage to control the VCO.

On-board voltage regulation is provided by I4, I14, I15 and I19 (see Figure 14-6).

The phase-locked-loop (PLL) circuitry (see Figure 14-7) includes the frequency synthesizer (I1), integrator (I2), loop filter (I3), VCO (Q3), dual modulus divider, and other circuitry (see Figure 14-7).

The PLL frequency synthesizer chip (I1) is programmed by the microcomputer. The three internal counters (N, A and R reference divider) are programmed for 25 kHz steps, dividing by 9,000 to 11,400 (this includes the 64/65 counter); the VCO is moved in 10 kHz increments. I8 and I9 divide the 90-114 MHz signal by 20 (I8 divides by 10 and I9 divides by 2).

The integrator integrates the + and - pulses coming out of the digital phase detector. The twin "T" notch filter (formed by R12, R13, R14, C39, C40, C41 and C42) is set to 10 kHz. The resulting dc control voltage is fed to the voltage variable capacitance diode (D3) in the voltage controlled oscillator (VCO) circuit.

The phase-detector, divide-by-500-counter, programmable counters, and control logic are all contained in one chip (I1).

Circuitry for the frequency selection switches, multiplexer and microcomputer is shown on the Schematic, Figure 14-8.

Four front panel frequency selection switch outputs are fed to tristate buffers that are used as multiplexers. The input switches provide BCD outputs to I16, I17 and I13. The 100s switch selects 100 kHz; the 10s switch selects 10 kHz; and the 1s switch selects 1 kHz increments. Switch S1 is 0/.5 and selects even kHz or 0.5 kHz. I13, I16 and I17 are TRI-STATE buffers that can have outputs of logic "0", "1" or "OFF". Their outputs are paralleled on the bus lines feeding the microcomputer. There are 16 inputs from the BCD switches, but only 8 input lines to the microcomputer. Therefore, data must be stored and sequentially read out into the microcomputer. I13, I16 and I17 function as a multiplexer converting parallel data to serial data.

I11 is the microcomputer and contains built-in RAM, ROM and EPROM. It must be programmed for a specific use. I12 accepts the BCD commands from the microcomputer and six decimal output lines for scanning the microprocessor. These scanning lines are inverted in I18 prior to driving the multiplexer. Q2 provides a logic "0" to pin 5 of J1 to signal an out-of-lock condition.

Other commands — baseband, receive, transmit, wave change, and wave change select — are also fed to the multiplexer. The contents of tristate buffers are scanned by the microprocessor to produce eight (8) command lines for the programmable counter. The lock detector output is also fed to the multiplexer and, if the VCO is not locked, the microprocessor generates an out-of-lock command.

Microcomputer I11 computes the proper divider numbers for I1 and loads them to I1, based on data that is read from the multiplexers (above).

14.6 Synthesizer Troubleshooting

Troubleshooting this module is not recommended. In the event there is a fault, return this module to the PULSAR factory.

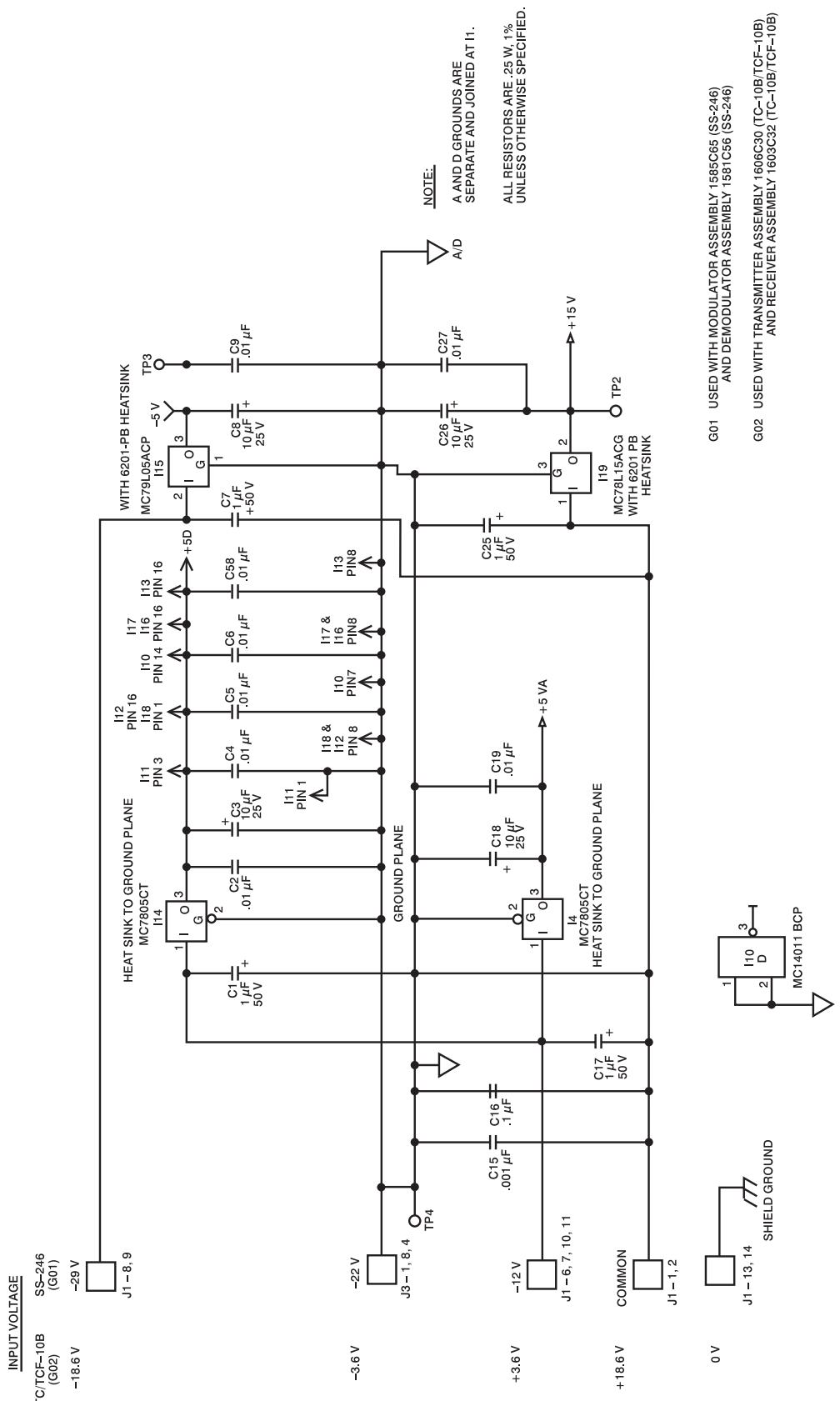


Figure 14–6. TC–10B/TCF–10B Synthesizer Schematic (1585C56S; Sheet 1 of 3).

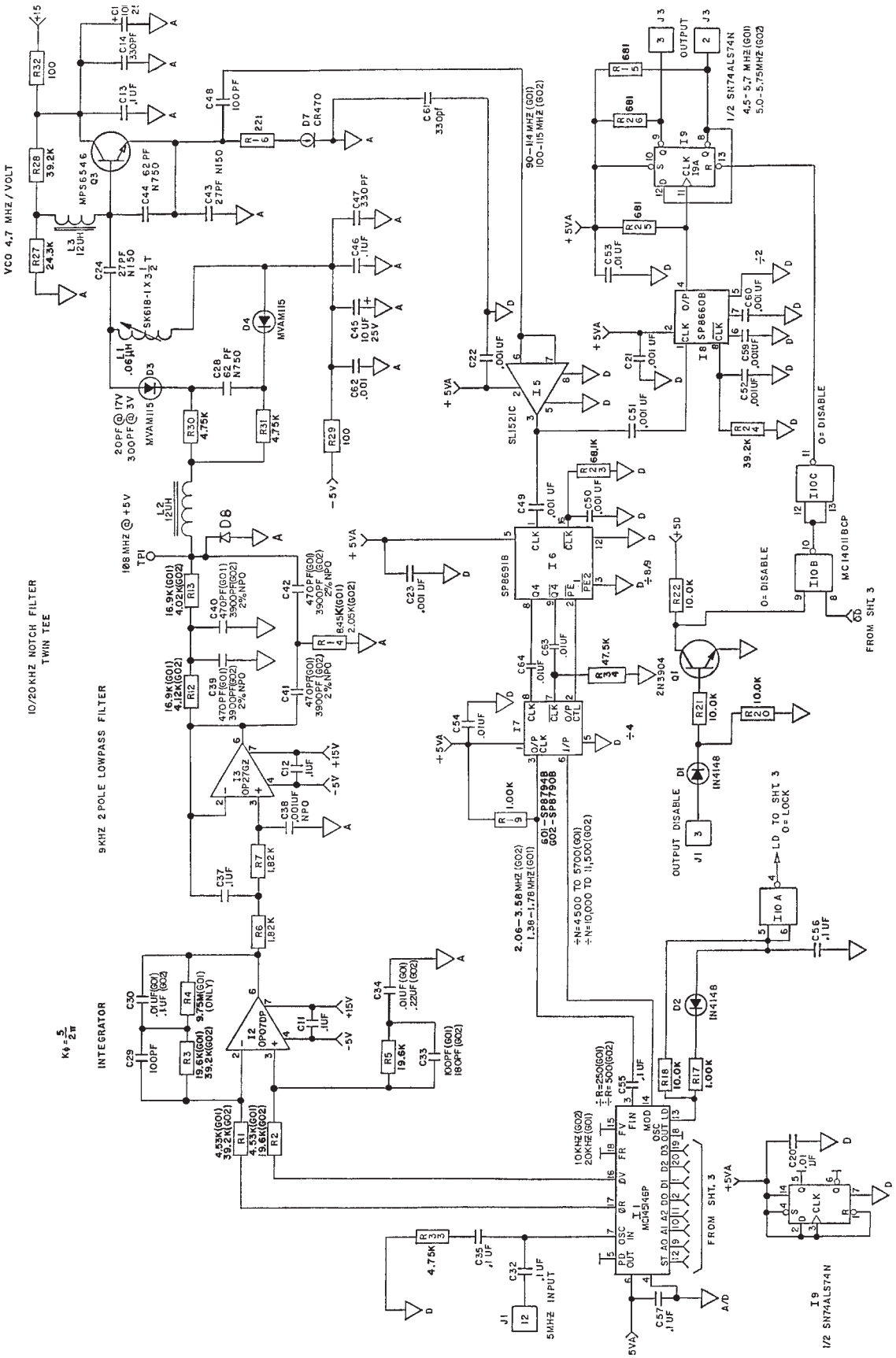


Figure 14–7. TC–10B/TCF–10B Synthesizer Schematic (1585C56S; Sheet 2 of 3).

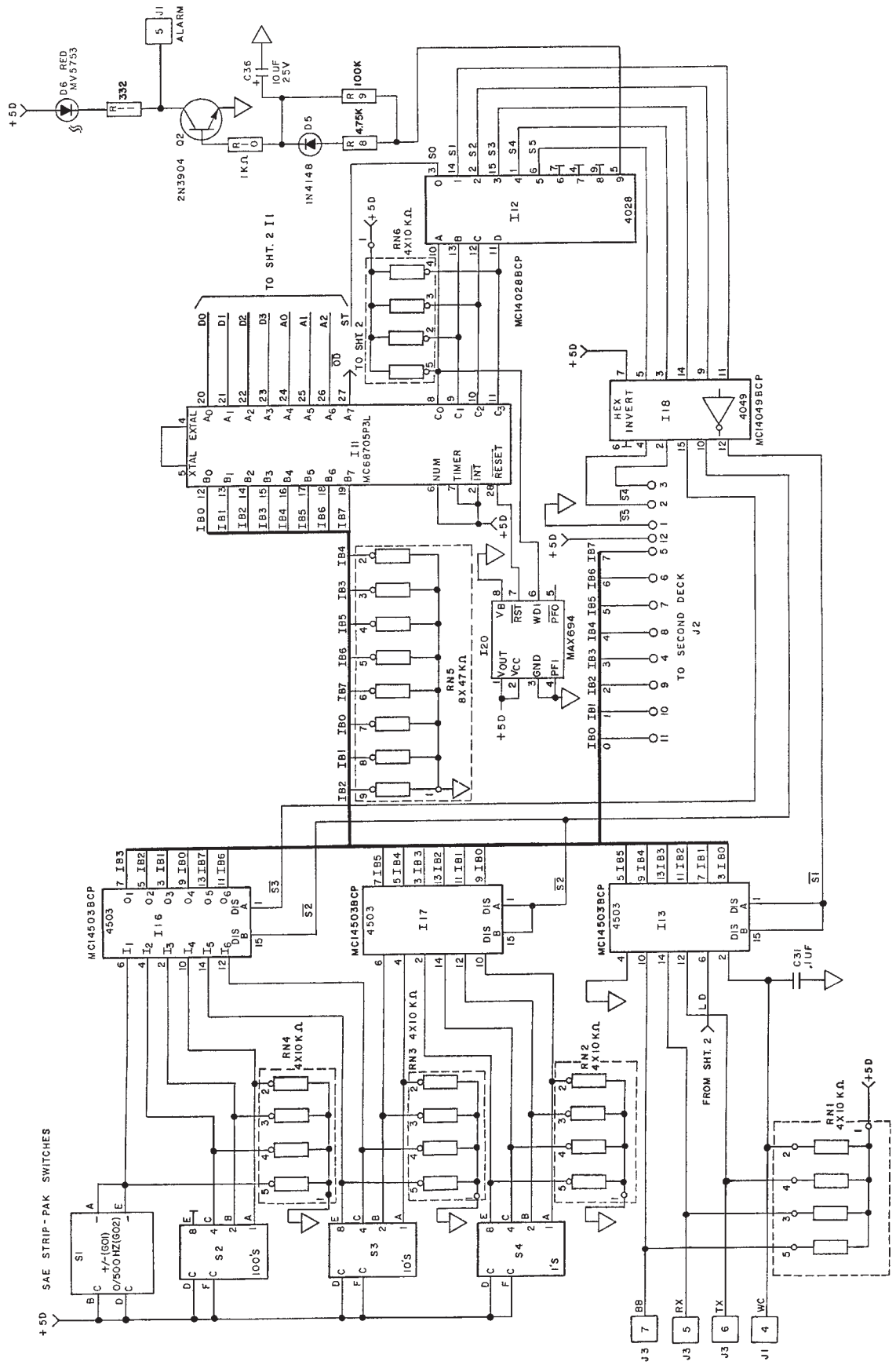


Figure 14–8. TC–10B/TCF–10B Synthesizer Schematic (1585C56S; Sheet 3 of 3).

Table 14–3. Synthesizer Module Components (1585C56).

Location	Style	Description	Group
CAPACITORS			
C1	CW1004MH76	1 µF 20% 50 V DIPPED TANTALUM	02
C2	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C3	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C4	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C5	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C6	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C7	CW1004MH76	1 µF 20% 50 V DIPPED TANTALUM	02
C8	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C9	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C10	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C11	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C12	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C13	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C14	CP3300KH65	330 pF 10% 50 V C0G MONO CERAMIC	02
C15	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C16	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C17	CW1004MH76	1 µF 20% 50 V DIPPED TANTALUM	02
C18	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C19	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C20	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C21	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C22	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C23	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C24	CP270AKL75	27 pF 10% 100 V N150 MONO CERAMIC	02
C25	CW1004MH76	1 µF 20% 50 V DIPPED TANTALUM	02
C26	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C27	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C28	CP620AKL75	62 pF 10% 100 V N750 MONO CERAMIC	02
C29	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	02
C30	CT1003JLZZ	0.1 µF 5% 100 V MET POLYESTER	02
C32	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C33	CP1800GH65	180 pF 2% 50 V C0G MONO CERAMIC	02
C34	CT2203JJ68	0.22 µF 5% 63 V MET POLYESTER	02
C35	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C36	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C37	CT1003JL68	0.1 µF 5% 100 V MET POLYESTER	02
C38	CP1001GH65	1000 pF 2% 50 V C0G MONO CERAMIC	02
C39	CP3901GH65	3900 pF 2% 50 V C0G MONO CERAMIC	02
C40	CP3901GH65	3900 pF 2% 50 V C0G MONO CERAMIC	02
C41	CP3901GH65	3900 pF 2% 50 V C0G MONO CERAMIC	02
C42	CP3901GH65	3900 pF 2% 50 V C0G MONO CERAMIC	02
C43	CP270AKL75	27 pF 10% 100 V N150 MONO CERAMIC	02
C44	CP620AKL75	62 pF 10% 100 V N750 MONO CERAMIC	02
C45	CW1005ME76	10 µF 20% 25 V DIPPED TANTALUM	02
C46	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02

Table 14–3. Synthesizer Module Components (Cont'd).

Location	Style	Description	Group
CAPACITORS (Cont'd)			
C47	CP3300KH65	330 pF 10% 50 V C0G MONO CERAMIC	02
C48	CP1000KH65	100 pF 10% 50 V X7R MONO CERAMIC	02
C49	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C50	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C51	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C52	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C53	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C54	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C55	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C56	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C57	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	02
C58	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C59	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C60	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C61	CP3300KH65	330 pF 10% 50 V C0G MONO CERAMIC	02
C62	CP1001ML65	1000 pF 20% 100 V X7R MONO CERAMIC	02
C63	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
C64	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	02
DIGITAL ICs			
I1	3533A95H01	MC145146P PLL FREQUENCY SYNTHESIZER	02
I6	3534A01H01	SP8691B 2-MODULUS (8/9) DIVDR 200MH	02
I7	9648A89H01	SP8790B DIV-BY-4 MODULUS EXTENDER	02
I8	3533A99H01	SP8660B DIVIDE-BY-10 200 MHz	02
I9	3535A66H01	SN74ALS74N DUAL D FLIP-FLOP	02
I10	3533A84H01	MC14011BCP QUAD 2-INPUT NAND	02
I12	3533A85H01	MC14028BCP BCD-DECIMAL DECODER	02
I13	3535A69H01	MC14503BCP HEX 3-STATE BUFFER	02
I16	3535A69H01	MC14503BCP HEX 3-STATE BUFFER	02
I17	3535A69H01	MC14503BCP HEX 3-STATE BUFFER	02
I18	3533A86H01	MC14049UBCP HEX INVERTER/BUFFER	02
I20	9654A53		
H02	MAX 694 CPA	02	
DIODES			
D1	836A928H06	1N4148 75 V 0.01 A	02
D2	836A928H06	1N4148 75 V 0.01 A	02
D3	3534A27H01	MVAM115 VARICAP 500 pF @ 1 V	02
D4	3534A27H01	MVAM115 VARICAP 500 pF @ 1 V	02
D5	836A928H06	1N4148 75 V 0.01 A	02
D7	3534A06H01	CR470 0.047 A CONSTANT CURRENT	02
INDUCTORS			
L1	3534A44H01	ADJ. 47	02
L2	3533A74H02	12 µH 10%	02
L3	3533A74H02	12 µH 10%	02

(Continued on next page.)

Table 14–3. Synthesizer Module Components (Cont'd).

Location	Style	Description	Group
LINEAR ICs			
I2	3533A96H01	OP07DP SINGLE OP-AMP (LO VOS)	02
I3	3533A97H01	OP27GZ SINGLE OP-AMP (LO NOISE)	02
I4	3533A90H01	MC7805CT POS VOLTREG 5 V 4% 1 A	02
I5	3533A98H01	SL1521C WIDEBAND AMP	02
I14	3533A90H01	MC7805CT POS VOLTREG 5 V 4% 1 A	02
I15	3533A93H01	MC79L05ACG NEG VOLTREG 5 V 5% 0.1 A	02
I19	3533A92H01	MC78L15ACG POS VOLTREG 15 V 5% 0.1 A	02
MICROPROCSSORS			
I11	1502B04G02	MICROPROCESSOR MC68705P3 (PROGRAMMED OPTOELECTRICS)	02
LEDs			
D6	3532A41H01	MV5753 LED RED	02
RESISTORS			
RN1	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	02
RN2	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	02
RN3	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	02
RN4	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	02
RN5	3533A81H02	8 COMM TERML 47 KILOHMS 2% SIP	02
RN6	3533A81H01	4 COMM TERML 10 KILOHMS 2% SIP	02
R1	RM3922FQA9	39.2 KILOHMS 1% 0.25 W METAL FILM	02
R2	RM1962FQA9	19.6 KILOHMS 1% 0.25 W METAL FILM	02
R3	RM3922FQA9	39.2 KILOHMS 1% 0.25 W METAL FILM	02
R5	RM1962FQA9	19.6 KILOHMS 1% 0.25 W METAL FILM	02
R6	RM1821FQB0	1.82 KILOHMS 1% 0.25 W METAL FILM	02
R7	RM1821FQB0	1.82 KILOHMS 1% 0.25 W METAL FILM	02
R8	RM4751FQB0	4.75 KILOHMS 1% 0.25 W METAL FILM	02
R9	RM1003FQ98	100 KILOHMS 1% 0.25 W METAL FILM	02
R10	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	02
R11	RM3320FQB1	332 OHMS 1% 0.25 W METAL FILM	02
R12	RM4121FQB0	4.12 KILOHMS 1% 0.25 W METAL FILM	02
R13	RM4021FQB0	4.02 KILOHMS 1% 0.25 W METAL FILM	02
R14	RM2051FQB0	2.05 KILOHMS 1% 0.25 W METAL FILM	02
R15	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	02
R16	RM2210FQB1	221 OHMS 1% 0.25 W METAL FILM	02
R17	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	02
R18	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	02
R19	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	02
R20	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	02
R21	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	02
R22	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	02
R23	RM6812FQA9	68.1 KILOHMS 1% 0.25 W METAL FILM	02
R24	RM3922FQA9	39.2 KILOHMS 1% 0.25 W METAL FILM	02
R25	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	02

RESISTORS (Cont'd)

Table 14–3. Synthesizer Module Components (Cont'd).

Location	Style	Description	Group
R26	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	02
R27	RM2432FQA9	24.3 KILOHMS 1% 0.25 W METAL FILM	02
R28	RM3922FQA9	39.2 KILOHMS 1% 0.25 W METAL FILM	02
R29	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	02
R30	RM4751FQB0	4.75 KILOHMS 1% 0.25 W METAL FILM	02
R31	RM4751FQB0	4.75 KILOHMS 1% 0.25 W METAL FILM	02
R32	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	02
R33	RM4751FQB0	4.75 KILOHMS 1% 0.25 W METAL FILM	02
R34	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	02
SWITCHES			
S1	3509A52H04	THUMBWHEEL 2 POLE 2 POS.	02
S2	3533A83H03	THUMBWHEEL BCD 5 POS.	02
S3	3533A83H02	THUMBWHEEL BCD 10 POS.	02
S4	3533A83H02	THUMBWHEEL BCD 10 POS.	02
TRANSISTORS			
Q1	3509A35H05	2N3904 40 V 0.2 A 0.625 W NPN	02
Q2	3509A35H05	2N3904 40 V 0.2 A 0.625 W NPN	02
Q3	3509A35H08	MPS6546 25 V 0.05 A 0.35 W NPN	02

USER NOTES

Chapter 15. Level Detector and CLI Module

Schematic	1606C34-7
Parts List	1606C34-7

Table 15–1. 1606C34 Styles and Descriptions.

Group	Description
G01	For Wideband (1,200 Hz) Receiver
G02	For Narrowband (600 Hz) Receiver

15.1 Level DET (Detector) And CLI Module Description

The Level Detector consists of a full-wave rectifier, low-pass filter, voltage comparator, and associated components; it functions as follows:

- Rectifies the 20 kHz output from the Receiver Module
- Measures the level of the 20 kHz signal
- Establishes a DETECT level as -15 dB or greater (when the 20 kHz signal is 0.177 Vp-p or greater), and provides indication thereof
- Establishes a MARGIN level as 0 dB or greater (when the 20 kHz signal is 1.0 Vp-p or greater), and provides indication thereof
- Provides LED indicators and relay circuits which activate based on received signals
- Provides +10 Vdc to the Receiver Output Module
- Provides positive output voltage to an optional Automatic Checkback Module, whenever the 20 kHz signal exceeds the detect level (0.177 Vp-p).
- Regulates system voltage (from +20 Vdc down to +15 Vdc).
- Provides for optional circuits as follows:
  - Log Amplifier
  - CLI Zero Adjust
  - Internal CLI Meter
  - External CLI Meter
  - Margin Alarm
- Provides a detected 20 kHz (squelch) signal to the optional Voice Adapter Module

15.1.1 Level Detector Control Panel

(This panel is shown in Figure 1-1.)

Operator displays are as follows:

LEDs

- MARGIN (D5)
- DETECT (D8)

Optional Internal CLI Meter

- MARGIN
- DETECT

Optional External CLI Meter

- MARGIN
- DETECT

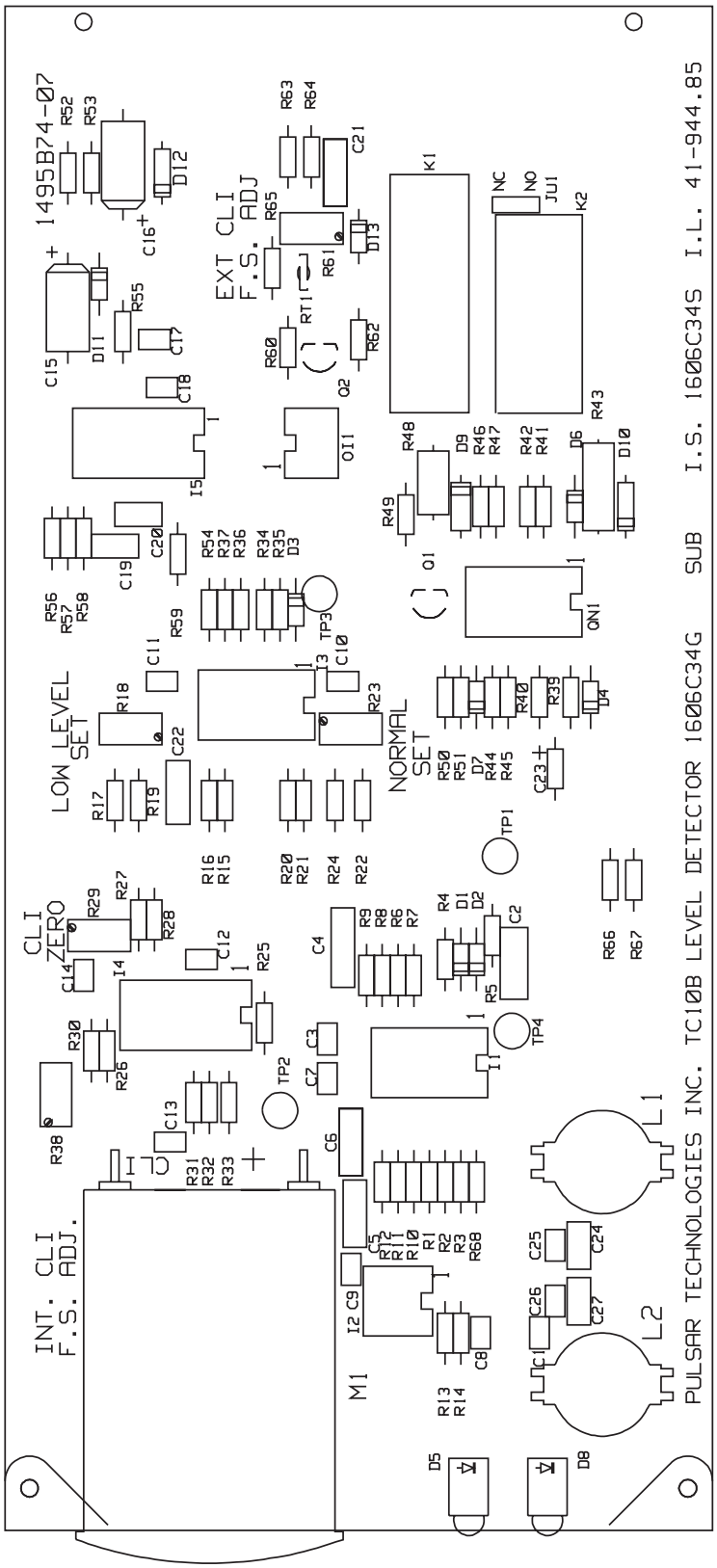
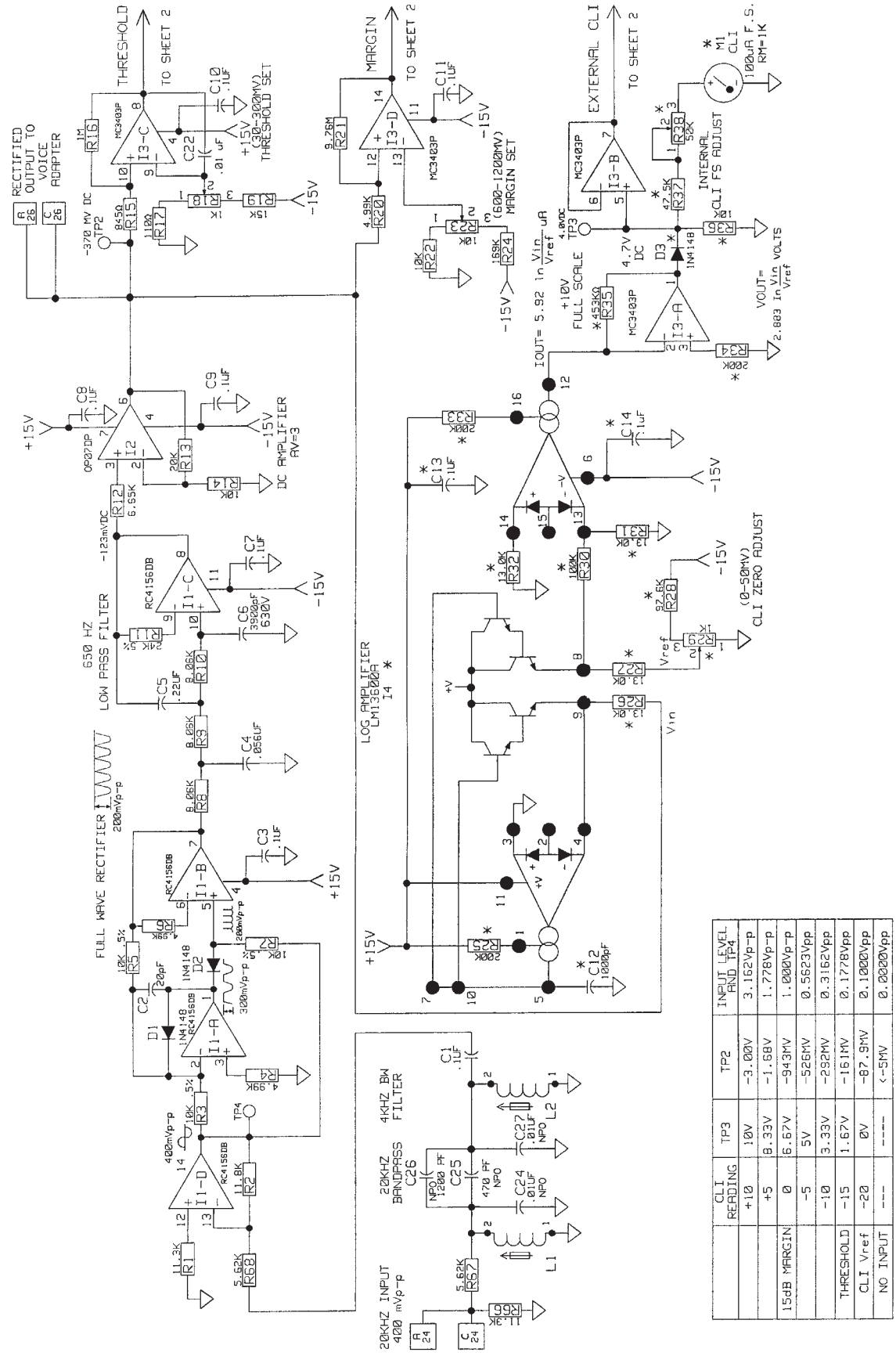


Figure 15–1. TC–10B Level Detector PC Board. (1495B74)



CLI READING	TP3	TP2	INPUT LEVEL AND TP4
+10	10V	-3.00V	3.162Vp-p
+5	8.33V	-1.68V	1.778Vp-p
15dB MARGIN	0	-943MV	1.000Vp-p
-5	5V	-526MV	0.5623Vpp
-10	3.33V	-293MV	0.3162Vpp
THRESHOLD	-15	-161MV	0.1778Vpp
CLI Vref	-20	-87.9MV	0.1000Vpp
NO INPUT	---	<-5MV	0.0000Vpp

Figure 15–2. TC–10B Level Detector and CLI Schematic (Sheet 1 of 2). (1606C34)

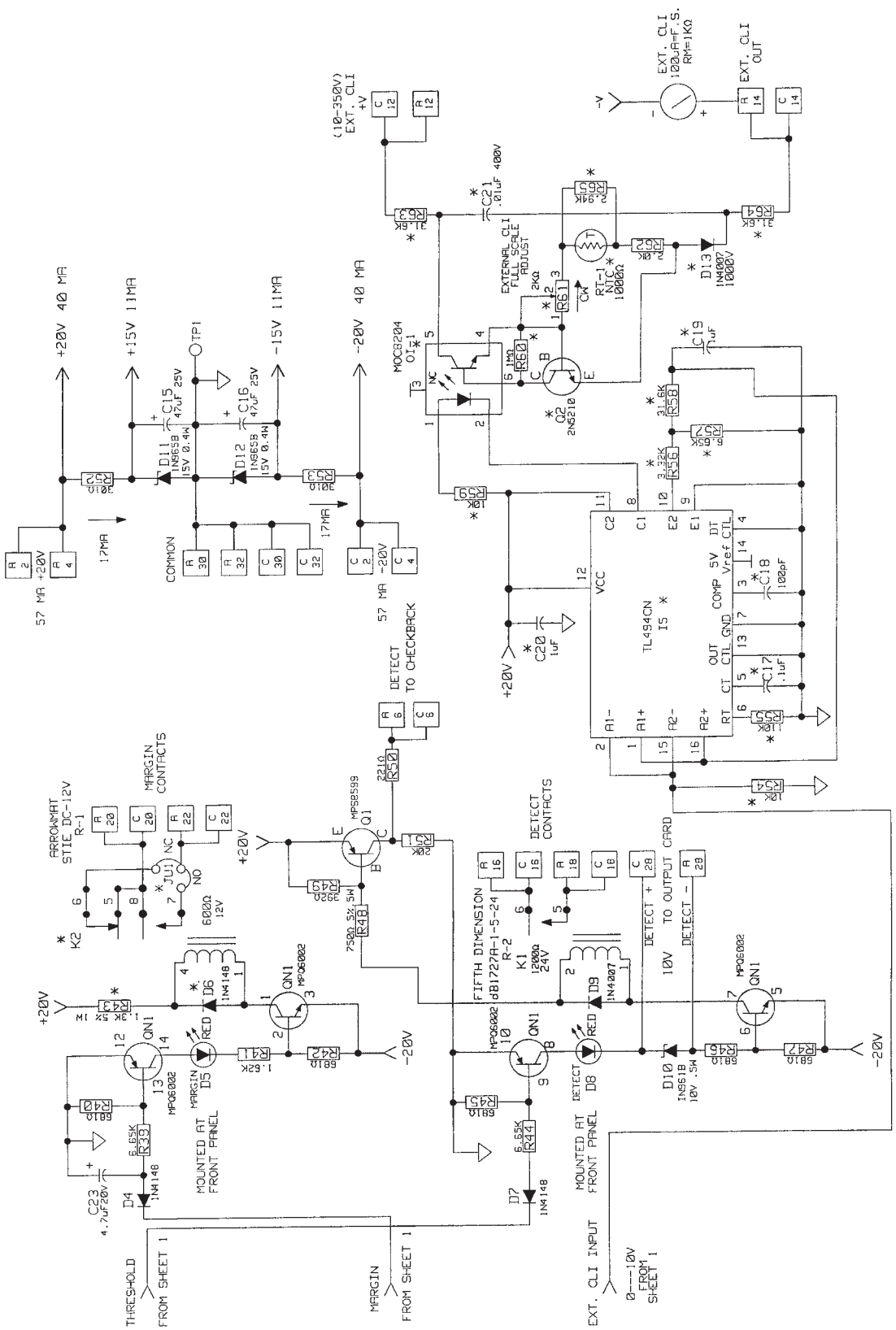


Figure 15–3. TC–10B Level Detector and CLI Schematic (Sheet 2 of 2). (1606C34)

15.1.2 Level Detector PC Board

(The Level Detector Board is shown in Figure 15-1.)

Operator controls are as follows:

Potentiometers

- CLI zero adjust for both internal and external CLI meters (R29)
- Internal CLI full-scale adjust (R38)
- External CLI full-scale adjust (R61)
- Adjusts threshold switching level (R18)
- Adjusts margin switching level (R23)

Jumper

Alternate contact states (NO/NC) for margin relay (JU1)

> NOTE
>
> **Jumper JU1 is shipped in the "NO" state.**

Test Points

TP1	Common
TP2	Rectified output voltage
TP3	Log output voltage
TP4	20 kHz signal

15.2 Level DET (Detector) And CLI Circuit Description

The Level Detector (see Figure 15-2 and Figure 15-3, Schematic 1606C34S) consists of a 20 kHz bandpass filter, full-wave rectifier, low-pass filter, voltage comparator and associated components. It functions as follows:

- Passes only 20 kHz + 2 kHz output from the Receiver Module; rectifies the 20 kHz output.
- Measures the level of the 20 kHz signal.
- Establishes a DETECT level as a signal level of 0.177 Vp-p or greater (which corresponds to 15 dB or greater), and provides indication thereof.
- Establishes a MARGIN level as a signal level of 1.0 Vp-p or greater (which corresponds to 0 dB or greater), and provides indication thereof.
- Provides LED indicators and relay circuits which activate based on received signals.
- Provides +10 Vdc to Receiver Output Module.
- Regulates system voltage (from ±20 Vdc down to ±15 Vdc).
- Provides for optional circuits as follows:
  - Log Amplifier
  - CLI Zero Adjust
  - Internal CLI Meter
  - External CLI Meter
  - Margin Relay
- Provides positive output voltage to an optional checkback Module, whenever the 20 kHz signal exceeds the threshold level 0.177 Vp-p.
- Provides a detected 20 kHz (squelch) signal to the optional Voice Adapter Module.

The 20 kHz input (from the Receiver Module) may be from 0 to 3.162 Vp-p; it drives a bandpass filter (L1, L2, C24, C25, C26, C27 and associated components), which is tuned to a center frequency of 20 kHz, with a 3 dB 4 kHz bandwidth. The 20 kHz input buffer (I1-D) has a gain sufficient to make up for the loss of the filter (which is about 6 dB). Full-wave rectification is provided by I1-A and I1-B with diodes D1, D2, and associated components. The output of I1-B is fed through a 650 Hz low-pass filter (R8, C4, R9, R10, I1-C, and associated components). The output of the filter is fed to DC amplifier I2.

The output of the DC amplifier drives the following:

- Voice adapter outputs (pins A26/C26)
- Two (2) Threshold detectors
- Optional logarithmic amplifier (I4)

The optional logarithmic amplifier (I4) is a dual operational, transconductance amplifier with linearizing diodes and buffers, driven from I2 through R26 (at I4 pin 9) to process the rectified Vdc from I2 (TP2), and convert it into log drive (at TP3) for the Internal or External CLI Meter.

The internal and external CLI ZERO ADJUST potentiometer (R29) is used to adjust the optional internal or external CLI meter reading at -20 dB, with a 20 kHz input of 0.1 Vp-p. The Internal CLI FULL SCALE potentiometer (R38) is used to adjust the internal CLI meter reading to +l0 dB, with a 20 kHz input of 3.162 Vp-p.

For example:

$$20 \text{ LOG } \left(\frac{3.1620}{.1000}\right) = 30 \text{ dB}$$

Table 15-2 lists a typical CLI meter reading for various 20 kHz input levels.

The external CLI drive circuit consists of buffer (I3-B), pulse width modulator (I5), optical isolator (OI-1), Q2, and associated components. The output of buffer I3-B is fed to I5 (see Figure 15-2 and Figure 15-3, Schematic). The pulse-width modulator control chip (I5) operates to cause proportional voltages between I5 pins 2 and 15 and OI-1 pins 1 and 2. This is accomplished by integrating the output pulses at I5 pin 10, and using the filtered Vdc as a reference that is fed to I5 pins 1 and 16. Given this condition, the Vdc at pins 1 and 16 will always be the same as the Vdc at pins 2 and 15. Because the output voltage at I5 pin 8 is 180° out-of-phase with the Vdc at I5 pin 10, the average Vdc through the input of OI-1 will always be proportional to the Vdc at I5 pins 2 and 15.

The clock pulse, determined by I5 (R55 and C17) is approximately 100 Hz. Unlike the classical power supply pulse-width modulator, many pulses can occur between clock pulses, because the internal flip-flop is not used. The optical isolator (OI-1) has an isolation voltage of 7500 Vdc and a transistor breakdown of 400 Vdc. OI-1, Q2, and associated components form a 100 μA current source that pulses "ON/OFF" through OI-1, producing a variable current for the CLI. Temperature compensation for the thermal charac-

Table 15–2. Typical CLI Meter Readings And Test Point Voltages For Various 20 kHz Input Levels.

	CLI READING	TP3	TP2	INPUT LEVEL AND TP4
	+10	10 V	-3.00 V	3.162 Vp-p
	+ 5	8.33 V	-1.68 V	1.77 Vp-p
15 dB MARGIN	0	6.67 V	-943 mV	1.000 Vp-p
	- 5	5 V	-526 m V	0.5623 Vp-p
	-10	3.33 V	-292 m V	0.3162 Vp-p
THRESHOLD	-15	1.67 V	-161 mV	0.1778 Vp-p
CLI V_{ref}	-20	0 V	-87.9 mV	0.1000 Vp-p
NO INPUT	—-	—-	<-5 mV	0.0000 Vp-p

teristics of OI-1 is provided by RT-1, R62, and R65. The External CLI FULL SCALE potentiometer (R61) is used to adjust the CLI meter reading to +10 dB, with a 20 kHz input of 3.162 Vp-p.

This meter will operate with 10 to 350 Vdc between pins A/C-12 and A/C-14.

Two circuits are used to drive- the LEDs (D8 and D5) and their respective relays (K1 and K2), as follows:

- Threshold (D8 and K1)
- Margin (D5 and K2)

The **threshold circuit** includes I3-C and potentiometer R18, which adjusts the switching level. A positive feedback resistor (R16) causes I3-C to behave as a switch. When voltage at TP2 becomes more negative than I3-C pin 9, then I3-C pin 8 switches to negative.

Similarly, the **margin circuit** includes I3-D, potentiometer R23, and resistor R21. When voltage at TP2 becomes more negative than I3-D pin 13, then I3-D pin 14 switches to negative.

The threshold output drives QN1-C/QN1-B; the margin output drives QN1-D/QN1-A. Whenever the input 20 kHz signal (pins A/C-24) is greater than .177 Vp-p or greater, threshold I3-C pin 8 goes negative, and QN1-C conducts, turning LED D8 "ON" to indicate the DETECT level is present (-15 dB or greater); QN1-B becomes saturated, and relay K1 is energized. Whenever the input 20 kHz signal is 1.0 Vp-p or greater, margin I3-D pin 14 goes negative, and QN1-D conducts, turning LED D5 "ON" to indicate the MARGIN level is present (0 dB or greater); QN1-A becomes saturated, and relay K-2 is energized.

The detect (+) and (-) output that is fed to the Receiver Output Module is from zener diode D10. Whenever the 20 kHz signal exceeds the threshold level, output pins A/C-28 will be at +10 Vdc.

The optional checkback system is signaled by Q1, and associated circuitry (see sheet 2), which provides a positive output voltage to pins A/C-6). Whenever the 20 kHz signal exceeds the threshold level, the Q1 signal will be high (logic "1").

Onboard voltage regulation and reverse polarity protection is provided by zener diodes D11 and D12. These diodes regulate ±20 Vdc (at 40 mA) input down to + 15 Vdc (at 11 mA). All bypass capacitors are connected to common pins A/C-30, A/C-32.

15.3 Level Detector And CLI Troubleshooting

Should a fault occur in this module, place the module on an extender board.

AC and DC signal levels are shown on the schematic (Figure 15-2 and Figure 15-3), for an input voltage of +10 dB (3.162 Vp-p).

Normal signal tracing with an oscilloscope and/or DC voltmeter will locate most faults. You may test diodes and other components conventionally with an ohmmeter.

Table 15–3. Level Detector Module Components (1606C34).

Location	Style	Description	Group
CAPACITORS			
C01	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C02	CR200AGV92	20 pF 2% 500 C DIPPED MICA	01,02
C03	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C04	CT5602JQ68	0.056 µF 5% 250 C MET POLYESTER	01,02
C05	CT2203JJ68	0.22 µF 5% 63 C MET POLYESTER	01,02
C06	CT3801JW68	3,800 pF 5% 630 C MET POLYESTER	01,02
C07	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C08	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C09	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C10	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C11	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01,02
C12	CP1001KL65	1,000 pF 10% 100 C X7R MONO CERAMIC	01
C13	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01
C14	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01
C15	CJ4705ME72	47 µF 20% 25 C MOLDED TANTALUM	01,02
C16	CJ4705ME72	47 µF 20% 25 C MOLDED TANTALUM	01,02
C17	CP1003MH65	0.1 µF 20% 50 C X7R MONO CERAMIC	01
C18	CP1000KH65	1 00 pF 10% 50 C X7R MONO CERAMIC	01
C19	CP1004MH54	1.0 µF 20% 50 C MONO CERAMIC	01
C20	CP1004MH54	1.0 µF 20% 50 C MONO CERAMIC	01
C21	CT1002JU68	0.01 µF 5% 400 C MET POLYESTER	01
C22	CT1502JU68	0.01 5 µF 5% 400 C MET POLYESTER	01,02
C23	CJ4704MD72	4.7 µF 20% 20 C MOLDED TANTALUM	01,02
C24	CP1002GH65	0.01 µF 2% 50 C C0G MONO CERAMIC	01,02
C25	CP4700GH65	470 pF 2% 50 C C0G MONO CERAMIC	01,02
C26	CP1201GL65	1,200 pF 2% 100 C C0G MONO CERAMIC	01,02
C27	CP1002GH65	0.01 µF 2% 50 C C0G MONO CERAMIC	01,02
DIODES			
D01	836A928H06	1N4148 75 C 0.01 A	01,02
D02	836A928H06	1N4148 75 C 0.01 A	01,02
D03	836A928H06	1N4148 75 C 0.01 A	01
D04	836A928H06	1N4148 75 C 0.01 A	01,02
D06	836A928H06	1N4148 75 C 0.01 A	01
D07	836A928H06	1N4148 75 C 0.01 A	01,02
D09	836A928H06	1N4148 75 C 0.01 A	01,02
D13	836A928H08	1N4007 1000 C 1 A	01
INDUCTORS			
L01	1495B88G01	INDUCTOR 5.48 MHZ ± 3%	01,02
L02	1495B88G01	INDUCTOR 5.48 MHZ ± 3%	01,02

Table 15–3. Level Detector Module Components. (Cont'd)

Location	Style	Description	Group
LINEAR ICs			
I01	3534A29H01	RC4156DB QUAD OP-AMP	01,02
I02	3533A96H01	OP07DP SINGLE OP-AMP (LO VOS)	01,02
I03	3537A40H01	MC3403P QUAD OP-AMP	01,02
I04	9646A34H01	LM13600A DUAL OP TRANSCOND AMP	01
I05	9645A92H01	TL494CN PULSE-WIDTH MODULATOR	01
QN01	3533A62H01	MPQ6002 QUAD PNP/NPN ARRAY 30 C 0.5 A	01,02
METERS			
M01	9646A95H01	100 μA F.S. RM=1 K	01
OPTOELECTRONICS			
D05	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01,02
D08	3508A22H01	RED LED- (EDGE MOUNT) 550-0406	01,02
OI01	774B936H02	MOC8204 OPTICAL ISOLATOR	01
POTENTIOMETERS			
R18	3534A25H04	1 K 25T TOP ADJ.	01,02
R23	3534A25H07	10 K 25T TOP ADJ	01,02
R29	3534A25H04	1 K 25T TOP ADJ.	01
R38	3534A25H06	50 K-OHM .5 W 25 TURN TOP ADJ. CERMET	01
R61	3534A25H04	1 K 25T TOP ADJ.	01
RELAYS			
K01	9644A13H01	DB1727-A-1-5-24	01.02
K02	1484B33H01	AROMAT TYPE ST1E-DC 12 C	01
RESISTORS			
R01	RM1132FQA9	11.3 KILOHMS 1% 0.25 W METAL FILM	01,02
R02	RM1182FQA9	11.8 KILOHMS 1% 0.25 W METAL FILM	01,02
R03	RM1002DQA8	10.0 KILOHMS 0.5% 0.25 W METAL FILM	01,02
R04	RM4991 FQB0	4.99 KILOHMS 1% 0.25 W METAL FILM	01,02
R05	RM1002DQA8	10.0 KILOHMS 0.5% 0.25 W METAL FILM	01,02
R06	RM4991 FQB0	4.99 KILOHMS 1% 0.25 W METAL FILM	01,02
R07	RM1002DQA8	10.0 KILOHMS 0.5% 0.25 W METAL FILM	01,02
R08	RM8061 FQB0	8.06 KILOHMS 1% 0.25 W METAL FILM	01,02
R09	RM8061 FQB0	8.06 KILOHMS 1% 0.25 W METAL FILM	01,02
R10	RM8061 FQB0	8.06 KILOHMS 1% 0.25 W METAL FILM	01,02
R11	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R12	RM6651FQB0	6.65 KILOHMS 1% 0.25 W METAL FILM	01,02
R13	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R14	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R15	RM8450FQB1	845 OHMS 1% 0.25 W METAL FILM	01,02
R16	RM1004FQ99	1.00 MEGOHMS 1% 0.25 W METAL FILM	01,02
R17	RM1100FQB1	1.10 OHMS 1% 0.25 W METAL FILM	01,02
R19	RM1502FQA9	15.0 KILOHMS 1% 0.25 W METAL FILM	01,02

(Continued on next page.)

Table 15–3. Level Detector Module Components. (Cont'd)

Location	Style	Description	Group
RESISTORS (Cont'd)			
R20	RM4991FQB0	4.99 KILOHMS 1% 0.25 W METAL FILM	01,02
R21	RM9764FQ99	9.76 MEGOHMS 1% 0.25 W METAL FILM	01,02
R22	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R24	RM1693FQ98	169 KILOHMS 1% 0.25 W METAL FILM	01,02
R25	RM2003FQ98	200 KILOHMS 1% 0.25 W METAL FILM	01
R26	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R27	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R28	RM9762FQA9	97.6 KILOHMS 1% 0.25 W METAL FILM	01
R30	RM1003FQ98	***NO ITEM DESCRIPTION'**	01
R31	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R32	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R33	RM2003FQ98	200 KILOHMS 1% 0.25 W METAL FILM	01
R34	RM2003FQ98	200 KILOHMS 1% 0.25 W METAL FILM	01
R35	RM4533FQ98	453 KILOHMS 1% 0.25 W METAL FILM	01
R36	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R37	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R39	RM6651FQB0	6.65 KILOHMS 1% 0.25 W METAL FILM	01,02
R40	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	01,02
R41	RM1621FQB0	1.62 KILOHMS 1% 0.25 W METAL FILM	01,02
R42	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	01,02
R43	RC1301J167	1.3 KILOHMS 5% 1 W CARBON COMP	01
R44	RM6651FQB0	6.65 KILOHMS 1% 0.25 W METAL FILM	01,02
R45	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	01,02
R46	RM6810FQBI	681 OHMS 1% 0.25 W METAL FILM	01,02
R47	RM6810FQB1	681 OHMS 1% 0.25 W METAL FILM	01,02
R48	RB7500JHL8	750 OHMS 5% 0.5 W CARBON FILM	01,02
R49	RM392AF0B4	39.2 OHMS 1% 0.25 W METAL FILM	01,02
R50	RM2210F0B1	221 OHMS 1% 0.25 W METAL FILM	01,02
R51	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01,02
R52	RM3010FQB1	301 OHMS 1% 0.25 W METAL FILM	01,02
R53	RM3010FQBI	301 OHMS 1 "/* 0.25 W METAL FILM	01,02
R54	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R55	RM1103FQ98	110 KILOHMS 1% 0.25 W METAL FILM	01
R56	RM3321FQB0	3.32 KILOHMS 1% 0.25 W METAL FILM	01
R57	RM6651FQB0	6.65 KILOHMS 1% 0.25 W METAL FILM	01
R58	RM3162FQA9	31.6 KILOHMS 1% 0.25 W METAL FILM	01
R59	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R60	RM1004FQ99	1.00 MEGOHMS 1% 0.25 W METAL FILM	01
R62	RM2671FQB0	2.67 KILOHMS 1% 0.25 W METAL FILM	01
R63	RM3162FQA9	31.6 KILOHMS 1% 0.25 W METAL FILM	01
R64	RM3162FQA9	31.6 KILOHMS 1% 0.25 W METAL FILM	01
R65	RM2941FQB0	2.94 KILOHMS 1% 0.25 W METAL FILM	01
R66	RM1132FQA9	11.3 KILOHMS 1% 0.25 W METAL FILM	01,02
R67	RM5621FQB0	5.62 KILOHMS 1% 0.25 W METAL FILM	01,02
R68	RM5621FQB0	5.62 KILOHMS 1% 0.25 W METAL FILM	01,02

Table 15–3. Level Detector Module Components. (Cont'd)

Location	Style	Description	Group
THERMISTORS			
RT01	185A211H14	1,000 OHM NTC	01
TRANSISTORS			
Q01	3509A35H09	MPS8599 80 C 0.5 A 0.35 W PNP	01,02
Q02	3509A35H12	2N5210 50 C 0.05 A 1.0 W NPN	01
ZENERS			
D10	186A797H07	1N961B 10 C 5% 0.4 W	01,02
D11	186A797H08	1N965B 15 C 5% 0.4 W	01,02
D12	186A797H08	1N965B 15 C 5% 0.4 W	01,02

USER NOTES

Chapter 16. Receiver (Solid State) Output Module

Schematic	CC30RXSM
Parts List	CC40RXSM

Table 16–1.
CC20-RXSMN-001 Styles and Descriptions.

Group	Description
001	Receiver (Solid State) Output

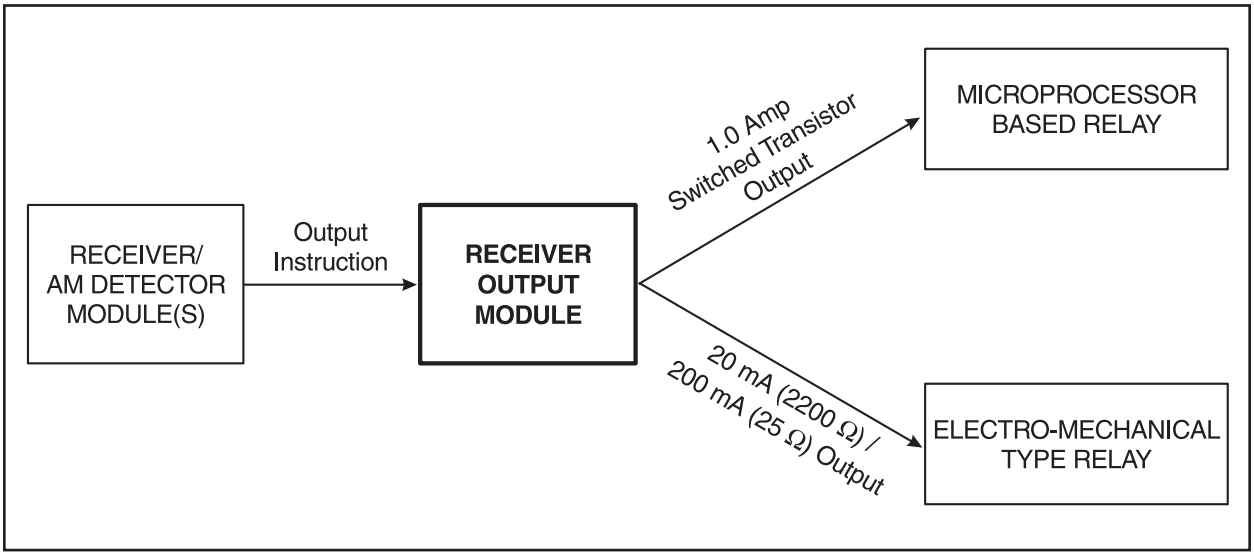


Figure 16–1. Receiver Output Module — Simplified Signal Flow Diagram.

16.1 Module Description

The TC–10B Receiver Output Module provides the appropriate outputs for both microprocessor based and electro-mechanical type relays. For a microprocessor based relay system, it provides two separate optically-isolated outputs between the carrier equipment and the relay. Both of these 1 A switched transistor outputs are solid-state circuits. For the older, electro-mechanical type relay systems, the module also provides either a 20 mA (2200 Ω) or 200 mA (25 Ω) output. All of these circuits may operate from voltage sources between 40 and 300 Vdc.

Figure 16-1 provides a simplified look at the Receiver Output Module's function. After the Receiver/AM Detector module(s) have received a signal (initiated by the relay attached to the carrier set at the other end) and determined that a carrier signal is present, they tell the Receiver Output Module to give an output to the (local) relay. The Receiver Output Module responds by giving the relay the appropriate output to provide blocking of the trip output. This lets the relay know the carrier is present so that it can ring the bell, sound the alarm, light the bulb, etc.

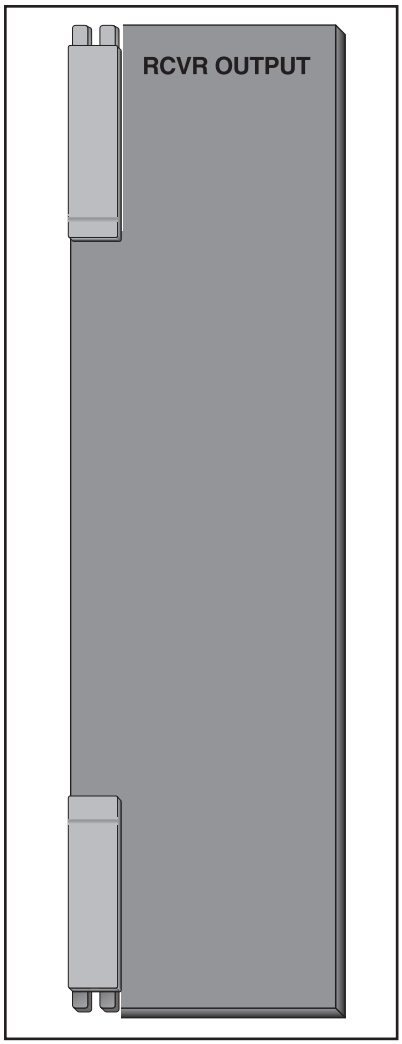


Figure 16–2.
Receiver Output Module
Front Panel.

The specific output the module gives to the relay is determined by the type of relay you are using and, for electro-mechanical type relays, how your relay circuit is set up.

Table 16-2 shows the connection options for both microprocessor based and electro-mechanical type relays. For further connection instructions for both types of relays, please see "Rear Panel Connections" later in this section.

16.1.1 Front Panel

As shown in Figure 16-2, the Receiver Output Module's front panel has no buttons, switches, LEDs, or other controls or indicators. This is because the module's function is automatic. The Receiver/AM Detector module(s) tell it when to send an output to the relay, and the type of output it sends is determined by the way the relay connection is configured.

16.1.2 Rear Panel Connections

You connect both microprocessor based and electro-mechanical type relays to the TB1 terminal block on the rear of the TC–10B carrier set. Table 16-2 shows the connection options for both types of relays. For diagrams showing the module's external connections, refer to Figure 3-6 in Chapter 3 and Figure 7-1 in Chapter 7.

Connecting a Microprocessor Based Relay

For a microprocessor based relay, connecting to the carrier set is as simple as connecting your relay wires to the correct connection screws on terminal block TB1.

To send OUTPUT #1 to the relay, connect the positive station battery lead to TB1-1 and the lead to the relay to TB1-2.

To send OUTPUT #2 to the relay, connect the positive station battery lead to TB1-4 and the lead to the relay to TB1-5.

Connecting an Electro-Mechanical Relay

For an electro-mechanical relay system, you have six connection options, depending on the (dc) voltage of your station battery and the desired output. Table 16-2 on the following page shows the correct terminal connections, jumper settings, and external resistor requirements for each connection option. The external resistors are provided on all sets supplied with this module.

Table 16–2. Output Table.

For use with Microprocessor-based Relays						
1 Amp Switched Transistor Output			Terminal Connections OUTPUT #1		Terminal Connections OUTPUT #2	
			TB1-1 (+) TB1-2		TB1-4 (+) TB1-5	
For use with Electro-Mechanical Relay Systems						
Carrier Aux Relay Position	Battery Voltage (Vdc)	External Resistor (ohms/watts)	Terminal Connections OUTPUT #1	JU1 Position	Terminal Connections OUTPUT #2	JU2
20 mA (2200 Ω)	48	none required	TB1-1 (+) & TB1-3	48	TB1-4 (+) & TB1-6	48
20 mA (2200 Ω)	125	3500/5	TB1-1 (+) & TB1-8	125/250	TB1-4 (+) & TB1-9	125/250
20 mA (2200 Ω)	250	9200/10 & 500/40	TB1-1 (+) & TB1-8	125/250	TB1-4 (+) & TB1-9	125/250
200 mA (25 Ω)	48	none required	TB1-1 (+) & TB1-3	48	TB1-4 (+) & TB1-6	48
200 mA (25 Ω)	125	none required	TB1-1 (+) & TB1-3	125/250	TB1-4 (+) & TB1-6	125/250
200 mA (25 Ω)	250	500/40	TB1-1 (+) & TB1-8	125/250	TB1-4 (+) & TB1-9	125/250

16.1.3 PC Board

The schematic for the Receiver Output Module's PC board is shown in Figure 16-3. The board has two jumpers labeled JU1 and JU2. If you are using electro-mechanical type relays, these jumpers must be set to match the station battery voltage for the relay circuit(s).

The options for JU1, which you set as part of the circuit for OUTPUT #1, are:

- 48 Vdc
- 125/250 Vdc

The options for JU2, which you set as part of the circuit for OUTPUT #2, are:

- 48 Vdc
- 125/250 Vdc

16.2 Circuit Description

As noted under "Module Description," the Receiver Output Module provides the appropriate outputs from the carrier set to both microprocessor based and electro-mechanical type relays. The relay circuits may operate from voltage sources between 40 and 300 Vdc.

This module is driven by the Receiver/AM Detector module(s) at pins A/C-26 (+) and A/C-28 (–). The module's two optical isolators (U1 and U2) provide the following outputs, which are available depending on the output connection (see Table 16-2):

- 20 mA
- 200 mA
- 1 A switched

Optical isolators U1 and U2 turn on together and share the following characteristics:

Isolation voltage: 7,500 Vdc

Transistor rating: 400 Vdc

The input from A-26 and A-28 energizes both optical isolators (U1 and U2). This initiates the circuit flow for both of the module's outputs. As described below, the two output circuits are virtually the same.

OUTPUT #1 Circuit Flow

The output from optical isolator U1 drives transistor Q1 to the ON state, which in turn drives transistor Q3 to the ON state. Transistor Q3 provides a 1 A output on A-14 and C-14 and a 20 mA/200 mA output on A-16 and C-16, with the station battery tied to A-12 and C-12.

Resistor R2, capacitor C1, and (metalized oxide) varistors M02 and M03 provide circuit protection against surges coming in from the outside world. Diode D1 provides reverse voltage protection — in case the outputs are connected backwards.

OUTPUT #2 Circuit Flow

The output from optical isolator U2 drives transistor Q2 to the ON state, which in turn drives transistor Q4 to the ON state. Transistor Q4 provides a 1 A output on C-20 and a 20 mA/200 mA output on A-22 and C-22, with the station battery tied to C-18.

Resistor R1, capacitor C2, and (metalized oxide) varistors M01 and M04 provide circuit protection against surges coming in from the outside world. Diode D2 provides reverse voltage protection — in case the outputs are connected backwards.

16.3 Troubleshooting

You can ensure the Receiver Output Module is getting the proper input from the Receiver/AM Detector module(s) by using the "Input Test" procedure described below. To make sure the module's outputs are correct, use the "Output Tests" procedure. To isolate and check faulty components, you can use your normal troubleshooting techniques.

16.3.1 Input Test

Use this procedure to verify that the Receiver Output Module is getting the proper input from the Receiver/AM Detector module(s). You will need the following:

- Extender board
- Digital volt meter

Preliminary Steps

1. Connect a power supply source (48, 125, or 250 Vdc) to the following rear panel terminals attached to the Receiver Output Module (with reference to TB7-2):
   - OUTPUT #1: TB1-1 (+)
   - OUTPUT #2: TB1-4 (+)
2. Place the Receiver Output Module on an extender board (see Figure 4-1).
3. Connect the digital volt meter to pins A/C-26 (+) and C-28 (–).

Input Test Procedure

Check the input coming from the Receiver/AM Detector module(s) at pins A/C-26 (+) and C-28 (–); potential voltage should be +10 Vdc.

1. Using the digital volt meter, measure the voltage level at pins A/C-26 (+) and C-28 (–). The potential voltage should be +10 Vdc.
2. Disconnect the digital volt meter.
3. Re-install the Receiver Output Module.

16.3.2 Output Tests

Use these tests to verify that the Receiver Output Module is providing the correct outputs for the relay system(s). You will need the following:

- Extender board
- Signal Generator (H/P 3325A)
- Simpson 260 (or equivalent) current meter
- Digital volt meter

Preliminary Steps

1. Remove the Keying Module from the chassis.
2. Connect a power supply source (48, 125, or 250 Vdc) to the following rear panel terminals attached to the Receiver Output Module (with reference to TB7-2):
   - OUTPUT #1: TB1-1 (+)
   - OUTPUT #2: TB1-4 (+)
3. Connect the Signal Generator (H/P 3325A) to the chassis at the UHF RF Input jack (J1) on the rear panel.
4. Place the Receiver Output Module on an extender board (see Figure 4-1).

Output Test Procedure

1. Set the Signal Generator to 250 kHz, at a level between 150 and 250 mVrms (The DETECT LED should be on.)
2. Use the digital volt meter to measure the voltage level at TB1-2 with TB7-2 as a reference. This voltage should be the same as the power supply source (48, 125, or 250 Vdc). Also, measure the voltage level at TB1-6 with TB7-2 as a reference. This should be the same as the power supply source (48, 125, or 250 Vdc).

Table 16–3. Receiver Output.

Terminal	Resistor Value (ohms/watt)	Battery Voltage (Vdc)	JU1/JU2 Position	Current limit (mA)
TB1-3	2200/2	48	48	20
TB1-8	2200/2	125	125/250	20
TB1-8	2200/2	250	125/250	20
TB1-3	25/5	48	48	200
TB1-3	25/5	125	125/250	200
TB1-8	25/5	250	125/250	200
TB1-6	2200/2	48	48	20
TB1-9	2200/2	125	125/250	20
TB1-9	2200/2	250	125/250	20
TB1-6	25/5	48	48	200
TB1-6	25/5	125	125/250	200
TB1-9	25/5	250	125/250	200

3. Remove the input signal, ensuring that the output level drops out.
4. Load down the output by connecting the appropriate resistor, as shown in Table 16-3.
5. Insert a current meter (Simpson 260 or equivalent) in the circuit by connecting the meter across the open switches on the card extender for pins C/A 16 for OUTPUT #1 and C/A 22 for OUTPUT #2.
6. Current readings should be 16 to 30 mAdc for a 2,200 ohm resistor and 160 to 230 mAdc for a 25 ohm resistor.
7. Disconnect the Signal Generator from the jack (J1) on the rear panel.
8. Re-install the Keying Module.

Table 16–4. Receiver (Solid State) Output Module Components (CC40RXSM).

Location	Style	Description	Quantity
CAPACITORS			
C1-2	CE1003JU25	0.1 μF, 5%, 400 V MET. POLYESTER	2
CONNECTORS			
J1	9646A11H02	32 PIN DIN, DUAL ROW	1
DIODES			
D1-2	188A342H23	1N5408, RECTIFIER	2
EJECTORS			
	1355D57H01	NYLON	2
HEADERS			
J2-3	9640A47H01	3 POSITION, 1 ROW STRAIGHT	2
JUMPERS			
(J2-3)	3532A54H01	BLUE CLIP, 2 POS.	2
NUTS			
(J1)	877A219H02	# 2-56 HEX	2
PANELS			
	1606C46H27	RCVR OUTPUT FRONT PANEL	1
PC BOARD			
	CC50-RXSMN	RCVR OUTPUT	1
RELAYS			
U1-2	9656A08H01	AQV254H, PHOTOMOS	2
RESISTORS			
R1-2	RM100AFQB4	10 OHMS, 1%, 0.25 W METAL FILM	2
R3-4	RM1000FQB1	100 OHMS, 1%, 0.25 W METAL FILM	2
R5-6		390, 1%, 50 W, WIREWOUND W/ HEATSINK	2
R7-8	RM3010FQB1	301 OHMS, 1%, 0.25 W METAL FILM	2
R9-10		200, 1%, 25 W, WIREWOUND W/ HEATSINK	2
R11	RB6200JQB2	620 OHMS, 5%, 0.25 W CARBON FILM	1
ROLL PINS			
	9654A52H01	FOR BOARD EJECTOR	2

Table 16–4. Receiver (Solid State) Output Module Components. (Cont'd)

Location	Style	Description	Quantity
SCREWS			
(R5-6, R9-10)	877A266H04	# 4-40 X .313 BINDING HEAD	12
(J1)	877A257H05	# 2-56 X .375 BINDING HEAD	2
STANDOFFS			
(R5-6, R9-10)		# 4-40 X .250 ALUM. FEMALE FORCE-FIT	4
TRANSISTORS			
Q1-2	3532A45H22	MJE5731, PNP, 300 V	2
Q3-4	3532A45H23	BUL45, NPN,	2
VARISTORS			
MO1-4	3509A31H11	V275LA4, 275 Vac RMS, 369 Vdc	4
WIRES			
(R5-6, R9-10)	66111KA30T	10 INCHES OF #22 AWG, WHITE INS.	
ZENERS			
Z1-2	837A693H10	1N4371, 2.7 V, 10%, 0.5 W	2

(Continued on next page.)

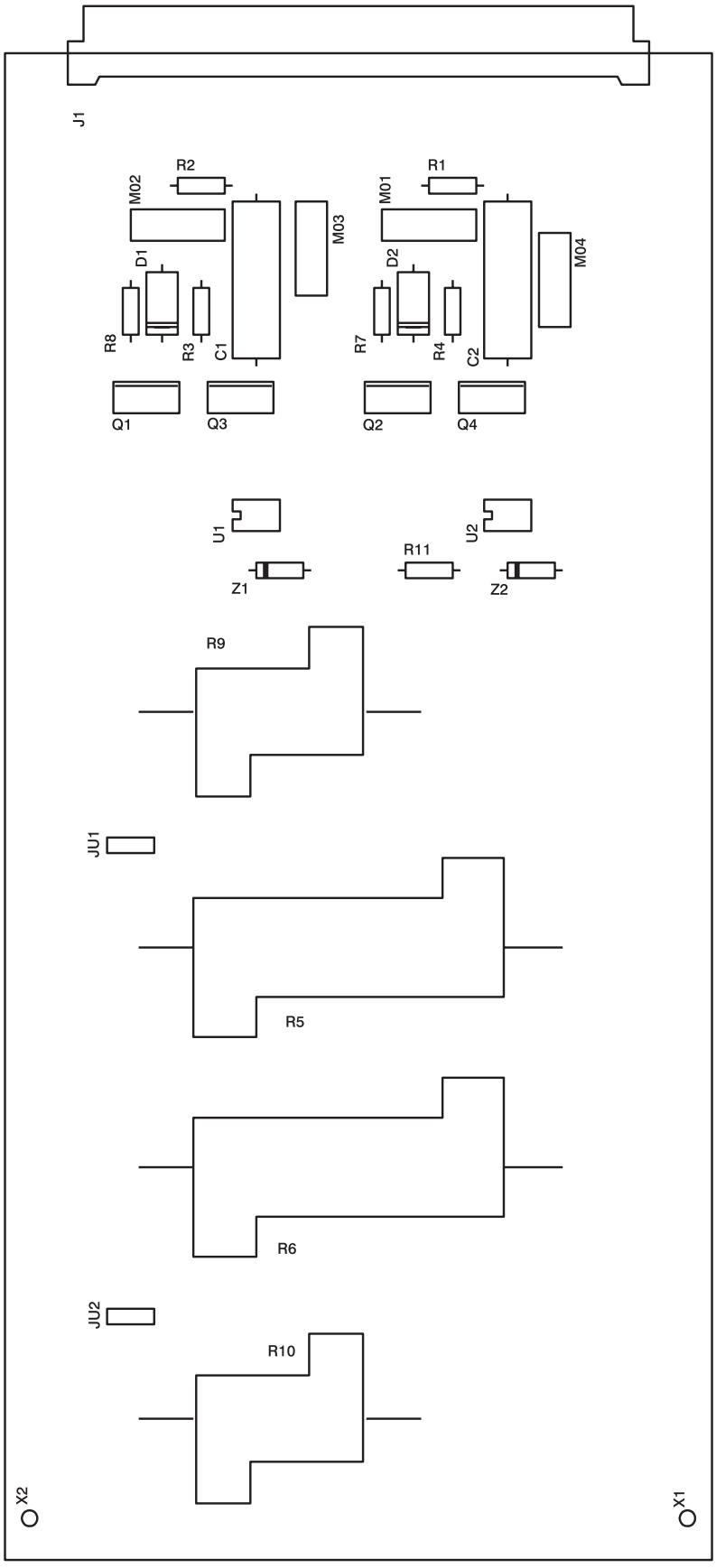


Figure 16–3. TC–10B Receiver Output PC Board. (CC50RXSM)

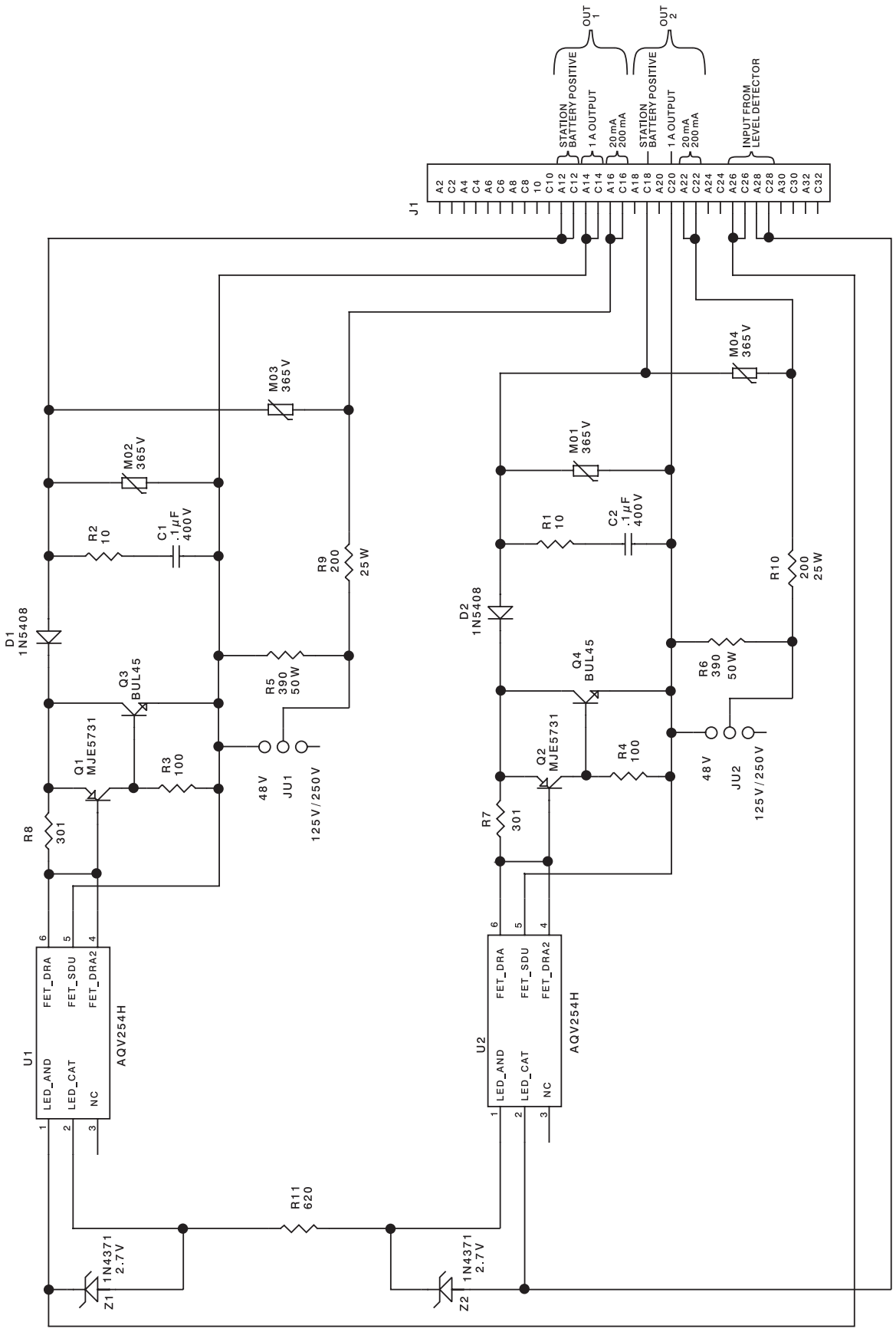


Figure 16–4. TC–10B Receiver Output Schematic. (CC30RXSM)

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USER NOTES

Chapter 17. Automatic Checkback System

Schematics:	1606C37-16 (Master) 1606C38-8 (Remote)
Parts Lists:	1606C37-16 (Master) 1606C38-8 (Remote)

The schematics listed to the left are shown both separately as Figures 17-18 through 17-22 (1606C37, Master Checkback Module) and Figures 17-23 through 17-25 (1606C38, Remote Checkback Module) and as part of larger diagrams in Figure 17-27 (2404F92), Figure 17-28 (2404F58), and Figure 17-29 (2404F93) at the end of this chapter.

Chapter Contents

17.1 Introduction

The Master and Remote Automatic Checkback Modules are designed for use both with the TC–10B "ON/OFF" carrier system and with other "ON/OFF" carrier systems.

Using these modules, you can initiate a test cycle, at regular programmed intervals, to determine whether or not your TC–10B (or other) carrier system's transmitters, receivers, and associated equipment are operable.

You can conduct two types of tests:

1) High-Level (for a carrier system using high power)

2) Low-Level (for a carrier system using low power)

The High-Level test maintains the transmitter at the high-level power you set (typically 10 watts for the TC–10B); the Low-Level test maintains the transmitter at the low-level power you set (typically 1 watt for the TC–10B). The TC–10B system leaves the factory with a full power setting of ten (10) watts, and a low power setting of one (1) watt.

If the tests result in any of the following three failure modes, you should troubleshoot your carrier system:

- A test is not functioning
- Tests are functioning, and the carrier system has passed the High-Level test(s) but has failed the Low-Level test(s)
- Tests are functioning, but the carrier system has failed a High-Level test

> NOTE
>
> Failure is indicated on the front panel LEDs and/or the events counter.

Table 17–1. Checkback Module Styles and Descriptions.

Style Number	Description
1606C37G01	Master Checkback Module with Events Counter
1606C37G02	Master Checkback Module w/o Events Counter
1606C38G01	Remote Checkback Module

17.1.1 System Assemblies

To use the Automatic Checkback System to test the TC–10B carrier system, insert a (Master or Remote) Checkback Module into the "Checkback" slot of the TC–10B chassis. If you are using the Automatic Checkback System to test other "ON/OFF" carrier sets, insert each (Master or Remote) Checkback Module into a separate "Digital Carrier Checkback" chassis.

17.1.2 Basic System Configuration

The basic system configuration includes a Master Checkback Module at the Master Carrier Station and a Remote Checkback Module at the Remote Carrier Station (see Figures 1-1 and 1-2 in Chapter 1).

You can order each Master Checkback Module either with an optional Events Counter (style number 1606C37G01) or without (style number 1606C37G02).

17.1.3 Other System Configurations

Different configurations of master and remote modules are available. In the minimum configuration, the Master Checkback Module communicates with a Remote Checkback Module on a two-terminal line. In the maximum configuration (see Figure 17-1), there are three different directions of signal transmission. The Master Checkback Module communicates with three different remote modules on a four-terminal line. Also, up to six different Slave Remote Modules (three "daisy chain" sets) can communicate with the Master Module through a Remote Module.

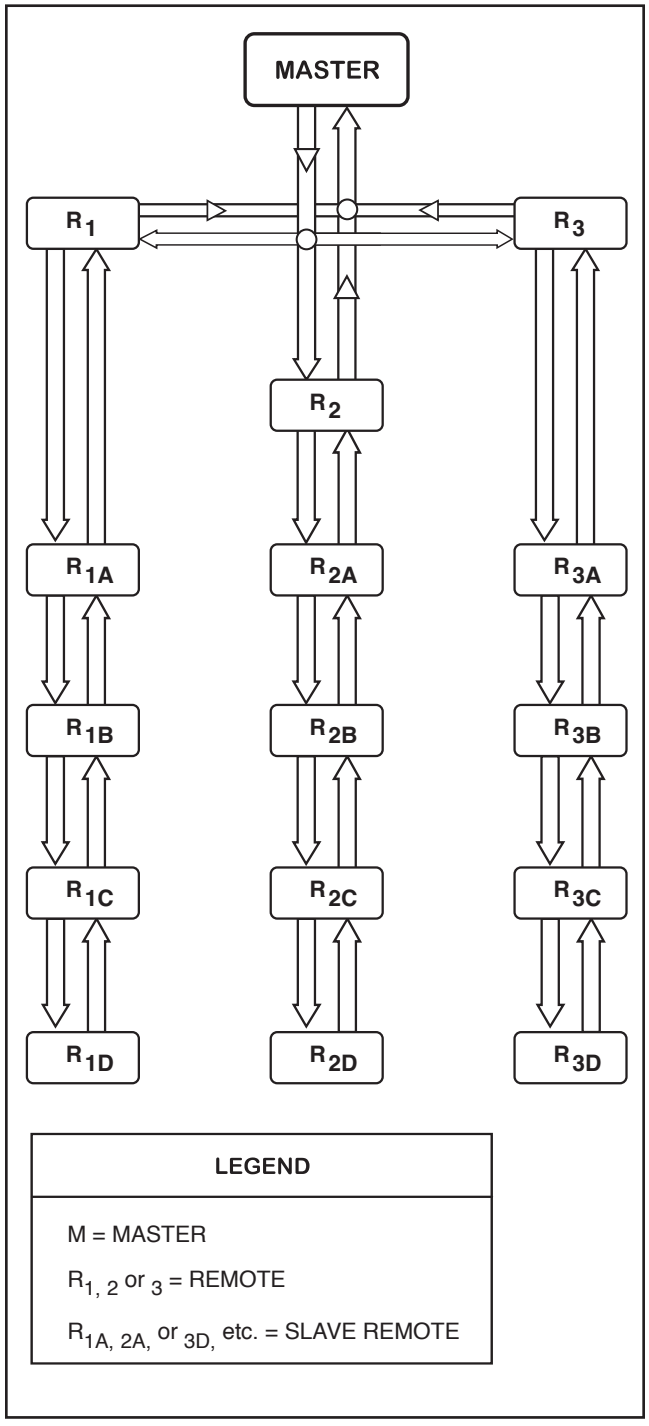


Figure 17–1.
Maximum Checkback Configuration. (9647A75)

17.1.4 Checkback Cycle Initiation

You can initiate a checkback cycle initiated in three ways:

1) Automatically, using the Interval Timer (see Figure 17-3)
2) Manually, by pushing the INITIATE push-button switch on either the Master or Remote Station front panel
3) By applying a dc voltage from the Supervisory Control circuitry or other remote control system

17.2 Checkback Operator Controls Summary

17.2.1 Master Checkback Operator Controls

(See the schematics in Figures 17-27, 17-28, and 17-29 at the end of this chapter.)

Jumpers

The following jumpers are on the Master Checkback Module:

JU1–JU6	Test Sequence
JU7	Clock Frequencies and Transmission Rates
JU8	Checkback Waiting (Response) Interval
JU9	Retry on Failure (Position B yields fewer errors)
JU10	Checkback Interval Timer
JU11	Stop after Failure
JU12	Alarm (Momentary/Seal-In)
JU13	Optional Events Counter
JU14	Auto Initiate (Block on Fail/Normal)
JU15	Supervisory Control Initiate

Switches

The following switches are provided as operator controls on the Master Checkback Module (see the figure references below):

S1	(TIMER RESET) Checkback Interval Timer Reset (Figure 17-2)
S2, S7, S8	Checkback Interval, 1-255 Hours (Figure 17-3 and Figure 17-11)
S3	(INITIATE) Manual Initiate (Figure 17-2)
S4	(EVENTS RESET) Optional Events Counter Reset (Figure 17-2)
S5	Transmit System Address (Figure 17-11)
S6	Receive System Address (Figure 17-11)

LEDs

- Low-Level Data (LL DATA)
- High-Level Data (HL DATA)
- Remote 1 Low-Level Test (LL1)
- Remote 1 High-Level Test (HL1)
- Remote 2 Low-Level Test (LL2)
- Remote 2 High-Level Test (HL2)
- Remote 3 Low-Level Test (LL3)
- Remote 3 High-Level Test (HL3)
- Optional LED display (3-digit)

17.2.2 Master Checkback Control Panel Explanations

The front panel of the Master Checkback Module (see Figure 17-2) contains two LEDs for indicating a test in progress:

HL DATA	This LED blinks when High-Level data is transmitted between Master and Remote
LL DATA	This LED blinks when Low-Level data is transmitted between Master and Remote

There are six LEDs that indicate which of three possible Remotes have ongoing tests and/or test failures:

1 (LL1)	"ON" (steady) during Low-Level test of Remote Module 1
2 (HL1)	"ON" (steady) during High-Level test of Remote Module 1
3 (LL2)	"ON" (steady) during Low-Level test of Remote Module 2
4 (HL2)	"ON" (steady) during High-Level test of Remote Module 2
5 (LL3)	"ON" (steady) during Low-Level test of Remote Module 3
6 (HL3)	"ON" (steady) during High-Level test of Remote Module 3

Each of the six LEDs (above) remain "ON" as an "alarm" if a test fails. The period of the alarm is as follows:

MOMENTARY—If the "momen-tary" jumper is selected, the LED remains "ON" for five (5) seconds after completion of the entire checkback cycle (the 5 seconds is based on a 192 Hz clock).

SEAL-IN—If the "seal-in" jumper is selected, the LED remains "ON" until the beginning of a new checkback cycle.

If the (optional) Events Counter is part of the system, the (optional) three-Digit LED Display shows the number of events which have been counted since the last reset. There are nine possible events (selected by jumper):

1) Good High-Level Tests
2) Good Low-Level Tests
3) Total Good Tests
4) High-Level Tests Performed
5) Low-Level Tests Performed
6) Total Tests Performed
7) High-Level Failures
8) Low-Level Failures
9) Total Failures

Decimal points appear on the three-Digit LED Display when the counter overflows beyond a count of 999 (∅ 1,000).

The Master Checkback Module front panel has three recessed pushbutton switches for manual operator controls:

S1 (TIMER RESET) Resets (to zero) the Interval Timer (in hours) between automatic checkback cycles.

S3 (INITIATE) Initiates a checkback cycle

S4 (EVENTS RESET) This optional switch resets the Events Counter to zero; the count is reflected on the three-digit LED display.

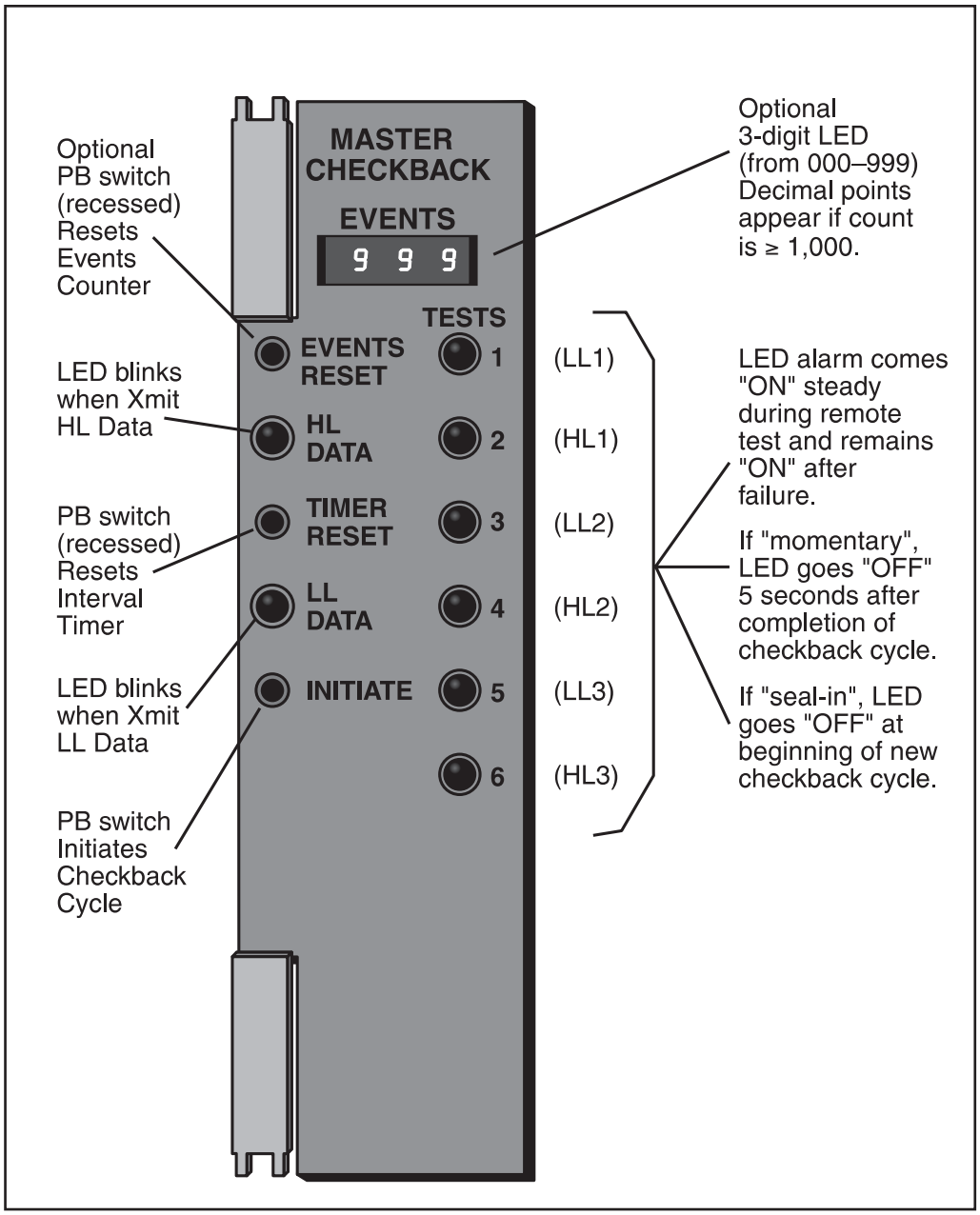
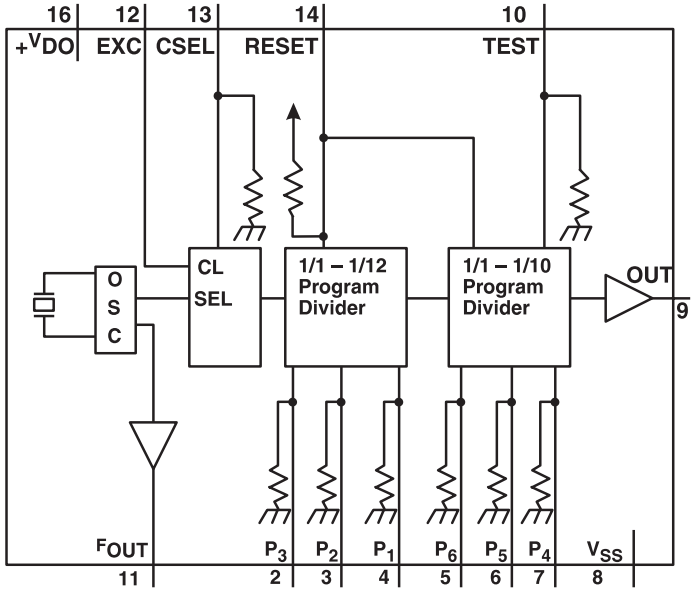


Figure 17–2.
Master Checkback Module — Front Panel. (Controls and Indicators)

Block Diagram of Programmable Oscillator (PXO-768)



Program Pin Settings										
		P4	0	0	0	0	1	1	1	1	D
		P5	0	0	1	1	0	0	1	1	E
		P6	0	1	0	1	0	1	0	1	F
P1	P2	P3									Master (JU7 settings) Remote (JU5 settings)
0	0	0	768 K	76.8 K	7.65 K	768	76.8	7.68	0.768	0.0768	
0	0	1	76.8 K	7.68 K	768	76.8	7.68	0.768	0.0768	0.00768	
0	1	0	384 K	38.4 K	3.84 K	384	38.4	3.84	0.384	0.0384	
0	1	1	256 K*	25.6 K	2.56 K	256	25.6	2.56	0.256	0.0256	
1	0	0	192K	19.2K	1.92K	192	19.2	1.92	0.192	0.0192	
1	0	1	153.6K**	15.36K	1.536K	153.6	15.36	1.536	0.1536	0.01536	
1	1	0	128K	12.8K	1.28K	128	12.8	1.28	0.128	0.0128	
1	1	1	64K	6.4K	640	64	6.4	0.64	0.064	0.0064	

A	B	C	Master (JU7 settings)	*33% Duty Cycle **40% Duty Cycle
B	A	C	Remote (JU5 settings)	"1" indicates the corresponding lettered jumper is on the board.

Switches S7 (8 position), S8 (4 position), and jumper JU10 on the Master Checkback auxiliary board enable you to set the checkback interval timer independently of the system clock (I35). Shown below are some settings for S7, S8, and JU10 and the resulting checkback intervals. You can then set switch S2 to the final checkback interval desired. S2 settings are in hours only when S7, S8, and JU10 are set to give one (1) pulse per hour. For example, if you were to set S2 to 8 for Example C, the checkback interval would be 24 hours. Setting S2 to 16 for Example A would yield 16 hours between checkback initiations. The standard factory settings are: clock speed = 192 Hz for 1200 Hz receiver unit, with S7, S8, and JU10 being set to Example A settings; and clock speed = 64 Hz for 600 Hz receiver unit, with S7, S8, and JU10 being set to Example D settings. If you slow the clock speed down to 64 Hz or lower, you must set switches S7 and S8 differently to produce one pulse each hour, per the table below:

Example	Clock Speed (Hz)	Pulses Per Hour (before division)	S8 Switch Positions (for I16)					S7 Switch Positions (for I15) "1" On = Down "0" Off = Up								÷ N	JU10 Setting A	JU10 Setting (Norm) B	÷ M	÷ NXM	Pulses Per Hour (after division) I18 – Pin 4
			*	1	2	4	8	*	1	2	4	8	1	2	4	8						
			S8	1	2	3	4	S7	5	6	7	8	1	2	3	4						
A	192	691,200		0	1	1	0		1	1	1	0	1	0	1	0	675		X	1024	691,200	1
B	192	691,200		1	0	1	1		1	0	1	0	0	0	0	0	1350		X	1024	1,382,400	1/2
C	64	230,400		0	1	1	0		1	1	1	0	1	0	1	0	675		X	1024	691,200	1/3
D	64	230,400		0	1	0	0		0	1	0	0	1	0	1	0	225		X	1024	230,400	1
E	6.4	23,040		0	1	1	1		0	0	1	0	0	0	0	0	1440	X		16	23,040	1
F	3.84	13,824		0	0	0	1		0	1	1	0	0	0	1	0	864	X		16	13,824	1
G	1.92	6,912		0	0	1	0		1	1	0	0	0	1	0	0	432	X		16	6,912	1
H	0.64	2,304		1	0	0	0		0	0	1	0	0	0	1	0	144	X		16	2,304	1

* = decimal equivalent number if switch is set to "1". Each group of 4 numbers adds up to be one of the digits of "N", with the S8 group being the most significant digit.

Figure 17–3. Master/Remote Checkback Clock Settings and Master Checkback Interval Timer Settings.

17.2.3 Remote Checkback Operator Controls

(See Figure 17-29 at the end of this chapter.)

Jumpers

The following jumpers are provided as operator controls on the Remote Checkback Module:

- JU1 Remote Module Number
- JU2 Daisy Chain or Normal
- JU3 Supervisory Control Initiate
- JU4 Voltage Level for Daisy Chain
- JU5 Clock Frequencies and Transmission Rates

Switches

The following switches are provided as operator controls on the Remote Checkback Module (see the figure references below):

- S1 Manual Initiate (the INITIATE push-button on the control panel, Figure 17-3)
- S2 Transmit System Address (on PC board, Figure 17-13)
- S3 Receive System Address (on PC board, Figure 17-13)

LEDs

- LL DATA Low-Level Data
- HL DATA High-Level Data

17.2.4 Remote Checkback Control Panel Explanations

The front panel of the Remote Checkback Module (see Figure 17-14) contains the following controls.

Two LEDs to indicate a test in progress:

- HL DATA This LED blinks when High-Level data is transmitted between Master and Remote
- LL DATA This LED blinks when Low-Level data is transmitted between Master and Remote

One recessed pushbutton switch:

- INITIATE (S1) Lets you manually initiate a checkback cycle.

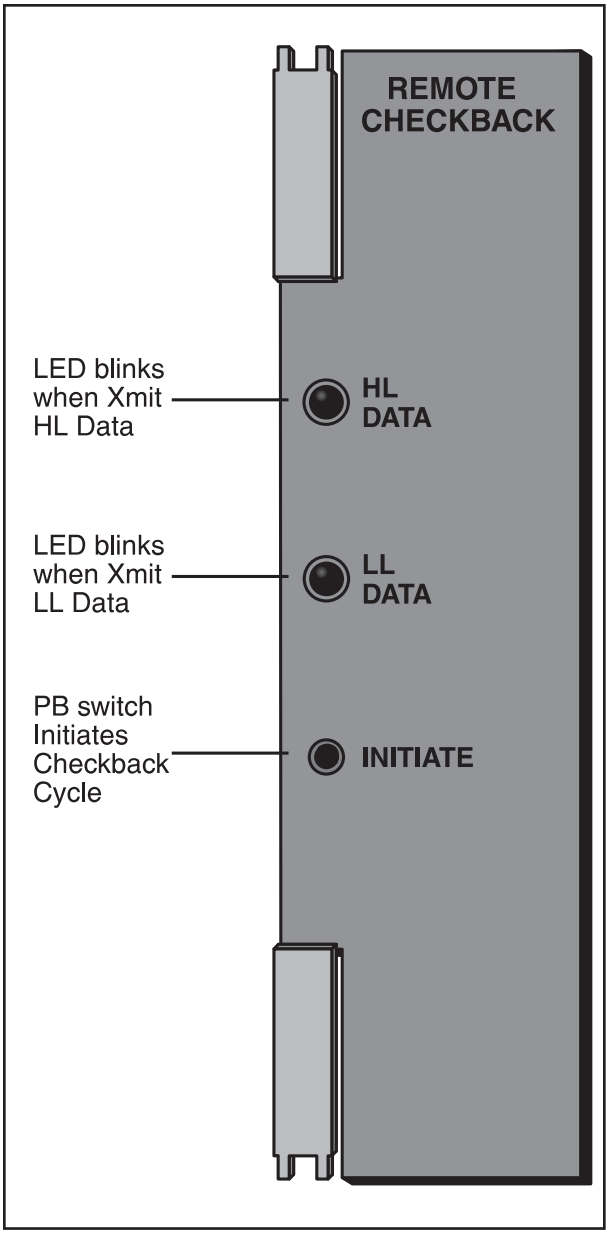


Figure 17–4. Remote Checkback Module — Front Panel. (Controls and Indicators)

17.3 Pre-Installation Setup Procedure

You must perform the following steps prior to installing the Checkback Modules for operation (see the PC boards and schematic diagrams according to the references below). The open position on DIP switches corresponds to logic zero. Down-logic "1"; Up-logic "0".

17.3.1 Master Checkback Setup Procedure

1. Using jumper JU15, select the voltage level at which Supervisory Control initiates the checkback cycle (see Figure 17-14):
   - 15 V
   - 48 V
   - 125 V
   - 250 V
2. Using switch S5, set the 5-bit binary Master System (XMIT) address (see Figure 17-11):
   - A0 (SW1)
   - A1 (SW2)
   - A2 (SW3)
   - A3 (SW4)
   - A4 (SW5)

> NOTE
>
> The Master System (XMIT) address must be identical to the Remote System (REC) address.

3. Using switch S6, set the 5-bit binary Master System (REC) address (see Figure 17-11).
   - A0 (SW1)
   - A1 (SW2)
   - A2 (SW3)
   - A3 (SW4)
   - A4 (SW5)

> NOTE
>
> The Master System (REC) address must be identical to the Remote System (XMIT) address (unless Slave Remotes are used—see 17.3.2, Steps 5 and 6).

4. Using the binary DIP switch S2, set the "automatic initiate interval timer" to a value from 1 to 255 hours (This is the time at which a new checkback cycle will begin. For clock speeds other than 192 Hz, you must set S7 and S8 to provide one (1) pulse per hour to S2 — see Figure 17-3, I15 and I16 switches S7 and S8.)

> NOTE
>
> Switch SW1 of binary DIP switch S2 is the least-significant bit (see Figure 17-11 and Figure 17-27).

5. Using the test jumpers (JU1 through JU6), select the Remote Stations, the types of tests at each Remote Station, and the order of all tests. For example (see Figure 17-11):
   - LL1 = JU1(A)
   - HL1 = JU2(B)
   - LL2 = JU3(C)
   - HL2 = JU4(D)
   - LL3 = JU5(E)
   - HL3 = JU6(F)
   - STOP = JU1, JU2, JU3, JU4, JU5, or JU6 Position G

> NOTE
>
> If you are running fewer than six tests, place the jumper that stops the test cycle at one position higher than the number of tests you are running. For example, if you are running the first five tests (LL1 through LL3), place jumper JU6 in the G position.

⚠ CAUTION

DO NOT PLACE MORE THAN ONE JUMPER IN THE STOP (G) POSITION.

6. If the (optional) "events counter" is part of the system, use JU13 to select the (test) events to be counted by the events counter (see Figure 17-11):
   1) Good High-Level Tests
   2) Good Low-Level Tests
   3) Total Good Tests
   4) High-Level Tests Performed
   5) Low-Level Tests Performed
   6) Total Tests Performed
   7) High-Level Failures
   8) Low-Level Failures
   9) Total Failures
7. Set the Checkback Response Interval.

   The "checkback response interval" is the time allocated for a transmitted test signal to be sent and a corresponding signal from a Remote to be received. If a signal is not received within the period of the checkback response interval, the test is considered a "Failure". Using jumper JU8, you must set the interval for either a system without Slave Remotes (1.5-second interval), or for the longest daisy chain configuration connected to one of the Remotes, as follows (see Figure 17-11):

   - One (1) second for each test response from one, two, or three Remotes, without Slave Remotes (i.e., no daisy chain). This is the time allocated for the data to be sent from the Master station to a Remote station and back to the Master station. If the data signal is not returned in 1.5 seconds, perform the next test (at any Remote in the system).
   - Two (2) seconds if there are two Slave Remotes (i.e., one daisy chain set).

     The additional 1.5 seconds is allocated for the data signal to return from the second Slave Remote.
   - Three (3) seconds if there are four Slave Remotes (i.e., two daisy chain sets).
   - Four (4) seconds if there are six Slave Remotes (i.e., three daisy chain sets).
8. Using jumper JU11, select the action which should follow a single test failure (see Figure 17-11):
   - Stop the test
   - Continue for the remainder of the checkback cycle
9. Using jumper JU9, select the appropriate test retry condition, after a test failure (see Figure 17-11):
   - No test retry (test run only once)
   - Retry the test (run the test twice to reduce the error rate)
10. Using jumper JU14, block or maintain the automatic initiation of a new checkback cycle, following the failure of a test (see Figure 17-11):
    - Block
    - Maintain (Normal)
11. Using jumper JU12, select the period of alarm activation following a single test failure (see Figure 17-11):
    - Momentary (Alarm stops after five seconds using the 192 Hz clock).
    - Seal-In (Alarm continues until the next checkback cycle starts).

17.3.2 Remote Checkback Setup Procedure

1. Using jumper JU3, select the voltage level at which supervisory control initiates the checkback cycle (see Figure 17-13):
   - 15 V
   - 48 V
   - 125 V
   - 250 V
2. Using jumper JU4, select the voltage level for daisy chain input (see Figure 17-13):
   - 15 V
   - 48 V
   - 125 V
   - 250 V
3. Using jumper JU1 at each Remote Module (if more than one Remote is used), select the number designated for the particular Remote Module, i.e., 1, 2, or 3 (see Figure 17-13).
4. Using jumper JU2, select the System Configuration type—with or without daisy chaining, i.e., without Slave Remotes (see Figure 17-1, Figure 17-5, and Figure 17-13):
   - Normal
   - Daisy Chain (see Figure 17-29 for optional use of the daisy chain function)
5. Using switch S2, set each 5-bit binary Remote System (XMIT) address, and each Slave Remote System (XMIT) address, if Slave Remotes are used (see Figure 17-13):
   - A0 (SW1)
   - A1 (SW2)
   - A2 (SW3)
   - A3 (SW4)
   - A4 (SW5)

NOTE

If you are not using Slave Remotes, the Remote System (XMIT) address must be identical to the Master System (REC) address. See Figure 17-7 for an example of an addressing scheme used to check four Slave Remotes. The Master Carrier (CXR) transmits address “10001”, which is received by Remote R1. Remote R1 transmits a different address “10011”, which bypasses Slave Remote R1A and is received at Slave Remote R1B. Similarly, Slave R1B transmits “10111” to Slave R1D; then R1D (“11111”) to R1C; R1C; (“01111”) to R1A; and R1A (“00111”) back to the Master.

6. Using switch S3, set each 5-bit binary Remote System (REC) address, and each Slave Remote System (REC) address, if you are using Slave Remotes (see Figure 17-13):
   - A0 (SW1)
   - A1 (SW2)
   - A2 (SW3)
   - A3 (SW4)
   - A4 (SW5)

NOTE

If you are not using Slave Remotes, the Remote System (REC) address must be identical to the Master System (XMIT) address. If you are using Slave Remotes, see Figure 17-5 for an example of an addressing scheme.

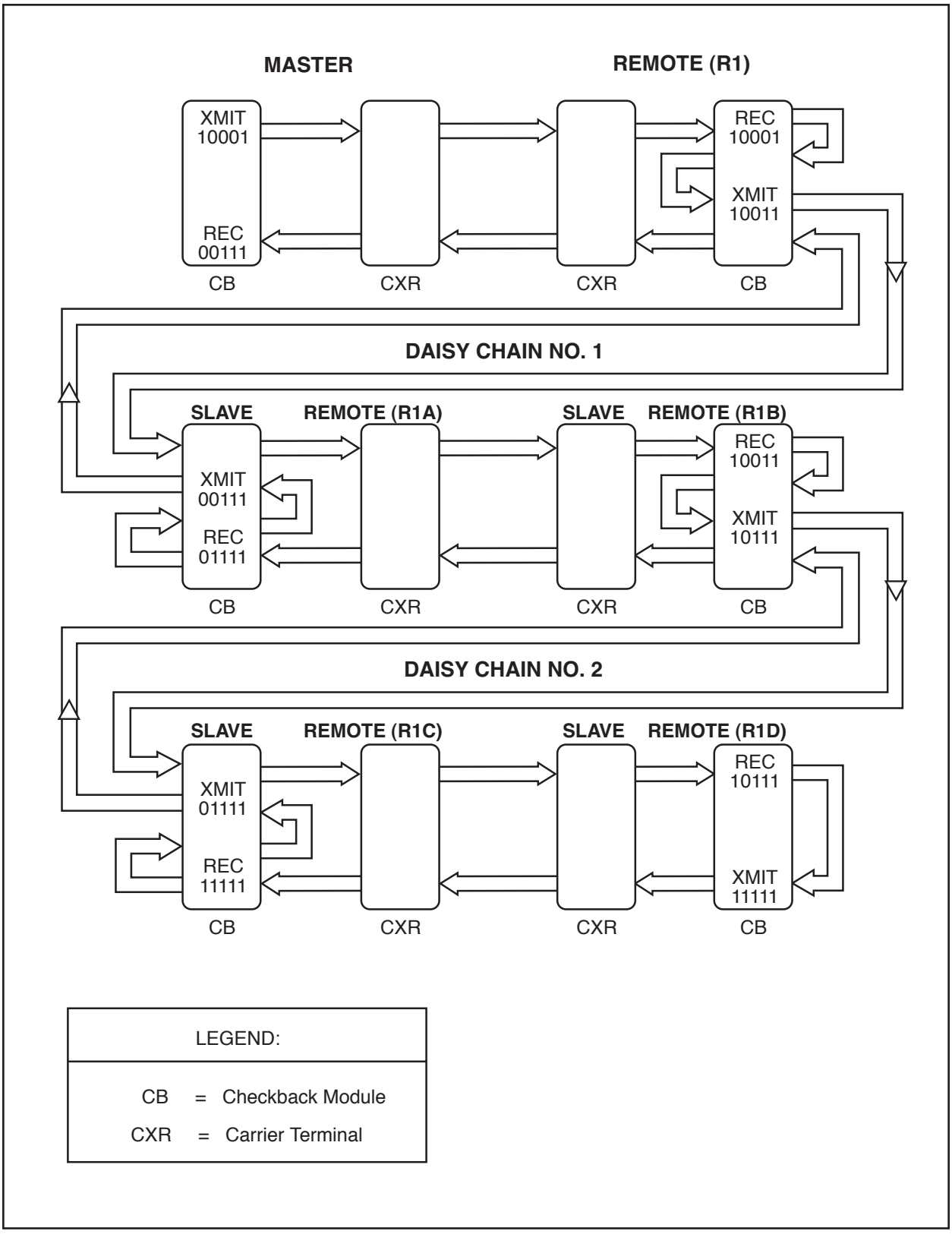


Figure 17–5.
Example of Matching Addresses Using Two Daisy-Chain Sets (Four Slave Remotes). (9647A74)

17.4 Installation

Make all external connections in accordance with the Wiring Diagram in this TC–10B System Manual (see Figure 3-5).

17.4.1 Factory Settings

The receiver bandwidth of the system using the checkback features determines the maximum speed of the checkback oscillator. The factory settings are shown in Table 17-2.

17.5 Start-Up Controls

The front panel of the Master Checkback Module is shown in Figure 17-2; the Remote Checkback Module in Figure 17-3.

Power "ON/OFF" Button

If the (Master, Remote or Slave Remote) Checkback Module is plugged into a TC–10B chassis, the power "ON/OFF" button is located on the Power Supply Module front panel.

> NOTE
>
> The power "ON/OFF" button is not a part of the operator controls shown in Figure 17-2 and Figure 17-4.

If the Checkback Module is plugged-into the DCB (stand-alone) Assembly (see the DCB Assembly manual), the power "ON/OFF" button is located on the DCB Assembly front panel.

Interval Timer Reset Pushbutton Switch (S1)

You can use the (interval) TIMER RESET pushbutton switch (S1) on the Master Checkback Module to reset the interval timer to zero (switch is recessed).

The interval timer is reset, automatically, when power is interrupted (or turned "OFF") at the Master Checkback Module.

Checkback Cycle

You can initiate the checkback cycle manually from either the Master or Remote Module by pressing the INITIATE pushbutton:

- Switch S3 at the Master Station
- Switch S1 at a Remote Station

> NOTE
>
> Neither switch resets the interval timer.

When dc voltage is applied to:

- Supervisory Control Initiate System (Remote)
- Other Remote Control System

the checkback cycle is initiated manually, as though you had pushed the Remote INITIATE pushbutton (switch S1).

> NOTE
>
> dc voltage does not reset the interval timer.

Table 17–2. Checkback Speed Vs. Receiver Bandwidths.

Receiver Bandwidth:	1200 HZ			600 Hz		
Jumper Positions	In	Out	Speed	In	Out	Speed
Master (JU7)	A, E, F	B, C, D	192 Hz	A, B, C, E,F	D	64 Hz
Remote (JU5)	B, E, F	A, C, D	384 Hz	A, B, E,F	C, D	128 Hz

17.6 Maintenance Controls

(Optional) Pushbutton Switch (S4)

The (optional) pushbutton switch (S4) on the Master Checkback Module is normally used on a periodic basis to reset the (optional) Events Counter.

> NOTE
>
> The (optional) Events Counter is not reset with loss of power or during power-on.

Jumper JU10 (on Master Checkback Module)

Jumper JU10, on the Master Checkback Module (see Figure 17-11), is used to expedite the system test only. It is not part of normal operating procedures. For very slow operating speeds, JU10 should be set in the A position (see Figure 17-3). For testing, use jumper JU10 to select a checkback interval sixty-four (64) times faster than hourly:

A. Faster Test

B. Normal Test

> NOTE
>
> These intervals are regulated by the Master clock (see Figure 17-3).

Jumper JU7 (on Master Checkback Module)

Jumper JU7 on the Master Checkback Module (see Figure 17-10), works in coordination with jumper JU5 on the Remote Checkback Module (see Figure 17-13), providing the following clock frequencies (f) and transmission rates (T.R.), as shown in Figure 17-3.

For special applications, such as driving relatively slow electro-mechanical devices, you can slow the clock down to less than 64 Hz. Figure 17-3 contains the block diagram of the clock oscillator (I35 on the Master and I20 on the Remote) and programmable frequency chart for the chip. JU7 on the Master Checkback and JU5 on the Remote are the jumpers you use to select the speed of the clock. These jumpers are solder-in jumpers. The current version of the board has six jumpers; A, B, C, D, E, and F. These are shown in Figure 17-3. Note that P1 and P2 are not the same for the Master and the Remote. (On the earlier boards that had only A, B, and C jumpers, a modification was made to the boards to slow down the clock speed.) Figure 17-3 also shows the settings of S7 and S8 on the Master Auxiliary board.

The time required for one bit increases as the clock frequency is reduced, as shown below:

Clock Frequency	Bit Time 0	Bit Time 1	Total (Milliseconds)
192 Hz	10.42	31.25	41.67
64	31.26	93.75	125.01
6.4	312.6	937.5	1250.1

The Checkback Interval time selected by S2 on the Master Checkback board is calibrated for one hour per bit up to 255 hours. This is based on a clock speed of 192 Hz. Switches S7 and S8 have been added to the Master Checkback in order to be able to change the division ratio of I15 and I16. Figure 17-3 illustrates the setting of S7 and S8 for a one hour per bit setting of S2 for clock speeds of 192, 64 and 6.4 Hz.

17.7 Programming

The checkback cycle operates under automatic program control when the sequence timer is activated.

17.7.1 Command Structure

Upon the initiation of a checkback cycle, the interval timer activates the first command.

Each command consists of one 8-bit digital word, as follows:

- The first three (3) bits contain data
- The remaining five (5) bits contain the system address

Data Structure

The three (3) bits used for data represent the six possible tests (LL1, HL1, LL2, HL2, LL3, and HL3) plus a Remote Initiate command; D0 and D1 combine to form a 2-digit binary code.

D0 1st Bit (Remote#)	D1 2nd Bit	HL/LL 3rd Bit (Remote#)	
0	0	0	Invalid Combination
1	0	0	Test Remote #1 Low-Level Test
0	1	0	Test Remote #2 Low-Level
1	1	0	Test Remote #3 Low-Level
0	0	1	Remote initiates a command to Master to begin automatic checkback cycle.
1	0	1	Test Remote #1 High-Level
0	1	1	Test Remote #2 High-Level
1	1	1	Test Remote #3 High-Level

17.7.2 System Address

Setting the 5-Bit Master System Address

To set the 5-bit Master System address, use the following address switches:

- Master System (XMIT) address switch S5, containing a 5-bit binary address:
  - A0 (SW1)
  - A1 (SW2)
  - A2 (SW3)
  - A3 (SW4)
  - A4 (SW5)
- Master System (REC) address switch S6, containing the same 5-bit binary address structure

Setting the 5-Bit Remote System Address

To set the 5-bit Remote System address, use the following address switches:

- Remote System (XMIT) address switch S2, containing the same 5-bit binary address structure as the Master System address.
- Remote System (REC) address switch S3, containing the same 5-bit binary address structure.

> NOTE
>
> The Remote System (XMIT) address must be identical to the Master System (REC) address; the Remote (REC) address the same as the Master (XMIT) address (see 17.3.2 Steps 5 and 6).

17.7.3 Transmission Structure

Each digital word is transmitted from the Master Station to the Remote Station and back to the Master Station, (for a security check) before the next digital word is transmitted.

> NOTE
>
> During transmission, the local checkback receiver is blocked from receiving.

17.7.4 Manually Initiating a Checkback Cycle

When the checkback cycle is initiated manually from the Master Station, it starts the sequence timer and activates the first command.

When the checkback cycle is initiated manually from a Remote Station, it sends a digital word to the Master Station, which starts the sequence timer and activates the first command.

17.8 Checkback Circuit Description

The TC–10B Automatic Checkback System comprises four circuit boards (see the figure references below):

- Master Main Board (shown by sections in Figures 17-18 through 17-21 and as a whole in Figure 17-27)
- Master Auxiliary Board (shown by sections in Figures 17-15 through 17-17 and as a whole in Figure 17-28)
- Master Display Board (shown enlarged in Figure 17-22 and reduced in Figure 17-28)
- Remote Board (shown by sections in Figure 17-23 through Figure 17-25 and as a whole in Figure 17-29)

The Master Checkback Module comprises three circuit boards (Main, Auxiliary, and Display), which are connected via connectors, as follows: JMP1 and JMP2 connect the Main Board to the Auxiliary Board, and JMP3 connects the Display Board to the Auxiliary Board. (For troubleshooting, use interconnect cables for JMP1 and JMP2.)

17.8.1 Master Checkback Main Board

The Main Board contains the power supply, power-up reset, clock oscillator, supervisory control and initiate circuitry, transmit circuitry, output circuitry, receive circuitry, backup battery, and reset switches.

Power Supply

(The power supply is shown at the upper right of the Main Board schematic, Figure 17-27.)

The power supply used is a 20 V to 5 V dc/dc switching power supply. The input +20 V is applied to connector pins A-2 and A-4 and is fed to modulator I36 through filter network C3, L1, C4, and C5. The pulse-width modulator chip (I36) oscillates at a frequency higher than 500 kHz (determined by R32 and C6). The pulse width is controlled by the output voltage applied to I36 pin 7 (VFB). As the output sample voltage (derived from R13/R14) increases above 5 V, the pulse width is narrowed and, as the output 5 V decreases below 5 V, the pulse width becomes wider. The actual switching from the 20 V input to the 5 V output is accomplished by Q1. The collector voltage of Q1 is filtered by C7, C8, C9, and L2. Q1 delivers power to the 5 V output when LX (pin 3) output from I36 goes low.

Power-Up Reset

(The power-up reset is shown at the upper left of the Main Board schematic, Figure 17-27.)

The power-up reset circuit consists of D15, R34, C10, R30, R29, and Q3. It prevents the transmitter from transmitting when power is initially applied to the unit. At this time, capacitor C10 discharges and forces the Q3 collector to go high until C10 is charged, creating a 1- to 3-second delay. The power-up reset circuit feeds the following circuits on the Main Board:

I42b pin 8 (set) Forces I42 pin 13 high, forcing LLTX and HLTX outputs to be low. Prevents transmitting during power-up reset.

I35 pin 10 (test) A high (logic 1) causes the clock to run 1,000 times faster than normal during the power-up reset interval (shown at the lower right of the Main Board schematic, Figure 17-27.)

The 192 kHz clock (normally 192 Hz) allows all the counters and registers in the checkback to be cleared during the power-up reset period.

The power-up reset circuit also feeds the Auxiliary Board's JMP2 pin 13 to I21 pin 12 (see Figure 17-28, lower right). This action causes I23 pin 13 (Q) to be low, preventing the generation of an events pulse.

Clock Oscillator

(The clock oscillator is shown at the lower right of the Main Board schematic, Figure 17-27.)

I35 is a programmable oscillator used to generate the 192-Hz (normal) clock frequency. JU7A, JU7B, JU7C, JU7D, JU7E, and JU7F are "0" ohm resistors that may be changed to increase or decrease the frequency of the clock. Normally, the clock is operated at 192 Hz (JU7A, JU7E, and JU7F only in). The pulse widths provided by the 192-Hz clock are satisfactory for the bandwidths of the system. However, the clock could be increased in frequency (usually for testing), or decreased in speed if bandwidth restrictions require. The available clock frequencies are shown in Figure 17-3.

It is important to note that the clock frequency of the Remote unit is always ***twice*** the frequency of the Master and, if the frequency of the Master is changed, the Remote must also be changed. For example, if the Master clock is 192 Hz, the Remote clock must be 384 Hz. A Master frequency of 128 Hz would require the Remote to be 256 Hz.

> NOTE
>
> The 256 Hz frequency (at the Master) cannot currently be used for operational purposes, as a 512 Hz frequency is unavailable at the Remote. The 768 Hz frequency is used for testing purposes only.

Initiate Circuitry

(The clock oscillator is shown at the lower right of the Main Board schematic, Figure 17-27.)

A checkback transmit signal may be initiated from supervisory control (manually), from the interval timer (automatically), or from the decoder. The initiate circuitry consists of JU15, I28, I31, I33, and I47. The supervisory initiate is applied between connector pins C-8 and C-10 and can be either 15 V, 48 V, 125 V, or 250 V, depending on the position of JU15. Current through D18 and the opto-isolator causes a logic "0" output from I28 pin 5 into "OR" gate I47. Manual initiate switch S3 also causes a logic "1" into I33. The auto initiate input comes from the Auxiliary Board on JMP2 pin 7.

If JU14 (see Figure 17-28, upper left) is in the BLOCK ON FAIL position, the LATCHED FAILURE input to I32 pin 9 from JMP2 pin 6 stops AUTO INITIATE.

An initiate pulse may be generated by the Remote Checkback Module if D0, D1, H/L, and VALID DATA commands from the Receiver are fed to I30 (a 4-bit magnitude comparator). This chip is configured to provide an output on pin 3 when the Remote Initiate code "001" and VALID DATA are

received. The 4-bit code "1100" represents VALID DATA, H/L, D1 and D0, respectively.

The initiate pulse is fed on JMP2 pin 1 to the Auxiliary Board, to I1 pin 15 (see Figure 17-28, lower left), which causes I1 to be scanning the test (LL1, HL1, LL2, HL2, LL3, and HL3). The Q0 output of I1 pin 3 generates the SEQUENCE INITIALIZE pulse. This pulse is fed back to the Main Board on JMP2 pin 12, and resets I31 so that it will be ready for the next initiate pulse.

Transmitter

(The transmitter is shown at the upper left of the Main Board schematic, Figure 17-27.)

The transmitter (encoder) consists of I37, I38, I39, I40, I41, and associated circuitry. It generates an 8-bit code consisting of five (5) address bits (selected by switch S5 on the Auxiliary Board) and three (3) data bits (D0, D1, and H/L). The three (3) data bits are generated by the sequencer (I1) on the Auxiliary Board (see Figure 17-28, lower left), and are fed to the Main Board on JMP1 pins 11, 9, and 10, respectively (see Figure 17-27, upper left). The five (5) address bits are fed from the Auxiliary Board (see Figure 17-28, upper left) to the Main Board on JMP1 pins 13, 16, 15, 14, and 12 (for A0, A1, A2, A3, and A4), respectively.

The three (3) data bits represent the six possible tests (LL1, HL1, LL2, HL2, LL3, and HL3) plus the remote initiate command.

The 8-bit code generated for each test provides a "1" for 31.25 milliseconds and a "0" for 10.42 milliseconds, for each bit period. These time intervals are based on a clock frequency of 192 Hz. The 8-bit code is started by the "start transmit" pulse (167 milliseconds) generated on the Auxiliary Board (see Figure 17-28, upper left) and fed to the Main Board (via JMP1 pin 8). The "start transmit" pulse resets I40, a 7-bit ripple counter (see Figure 17-27, upper left), as the TX BUSY line goes low, and I37A pin 3 begins delivery of 96-Hz clock pulses to I40 pin 1. The transmit continues until thirty-three (33) clock pulses are counted. The Timing Diagram (see Figure 17-6) illustrates the important wave shapes in the transmitter.

A static 8-bit shift register (I41) is shown in Figure 17-27, upper left. The parallel data—five (5) address bits and three (3) data bits—are shown (see Figure 17-6) as P1 through P8 and are shifted out serially from I41 pin 3. After the eight (8) bits are transmitted, I41 pin 9 becomes logic "1", and parallel data can be loaded into the register.

The best way of testing and troubleshooting the transmitter is to use a storage oscilloscope, because of the relatively low frame rate. If you synchronize the oscilloscope on I39A pin 10, you can use two probes to observe various data points in the transmitter circuitry.

Output Circuitry

(The output circuitry is shown at the upper right of the Main Board schematic, Figure 17-27.)

The output circuitry on the Main Board consists of QN1, QN2, Q2, K1, K2, K3, and associated components. The relay output for High-Level (HL) alarms is K1. It is driven by QN1 (9, 8, 10) and the LATCHED HL FAIL line from the Auxiliary Board (via JMP1 pin 4). The relay output for Low-Level (LL) alarms is K2. It is driven by QN1 (6, 7, 5) and the LATCHED LL FAIL line from the Auxiliary Board (via JMP1 pin 3). The events relay (K3) is driven by QN1 (2, 1, 3). The event to be monitored is selected by jumper JU13 on the Auxiliary Board (see Figure 17-28, lower right), and is fed to the Main Board via JMP1 pin 5 (EVENTS PULSE). K1, K2, and K3 all provide N.O. or N.C. contacts.

The HL data on the Main Board (see Figure 17-27, upper left), is transmitted via I38B pin 10 (LL) and I38C pin 4 (HL) and is fed to QN1 (13, 14, 12) and QN2 (6, 7, 5) (see Figure 17-27, upper right).

The LL data (see Figure 17-27, upper left) is transmitted to QN2 (2, 1, 3) and Q2 (see Figure 17-27, upper right). QN1 (13, 14, 12) drives the HL data LED (D13), Q2 drives the LL data LED (D10).

The HL key data is output from QN2 (9, 8, 10) and fed to connector pin A-6. The LL Key data is output from QN2 (13, 14, 12) and fed to connector pin A-28. Note that the HL and LL key outputs are +15 to +17 Vdc.

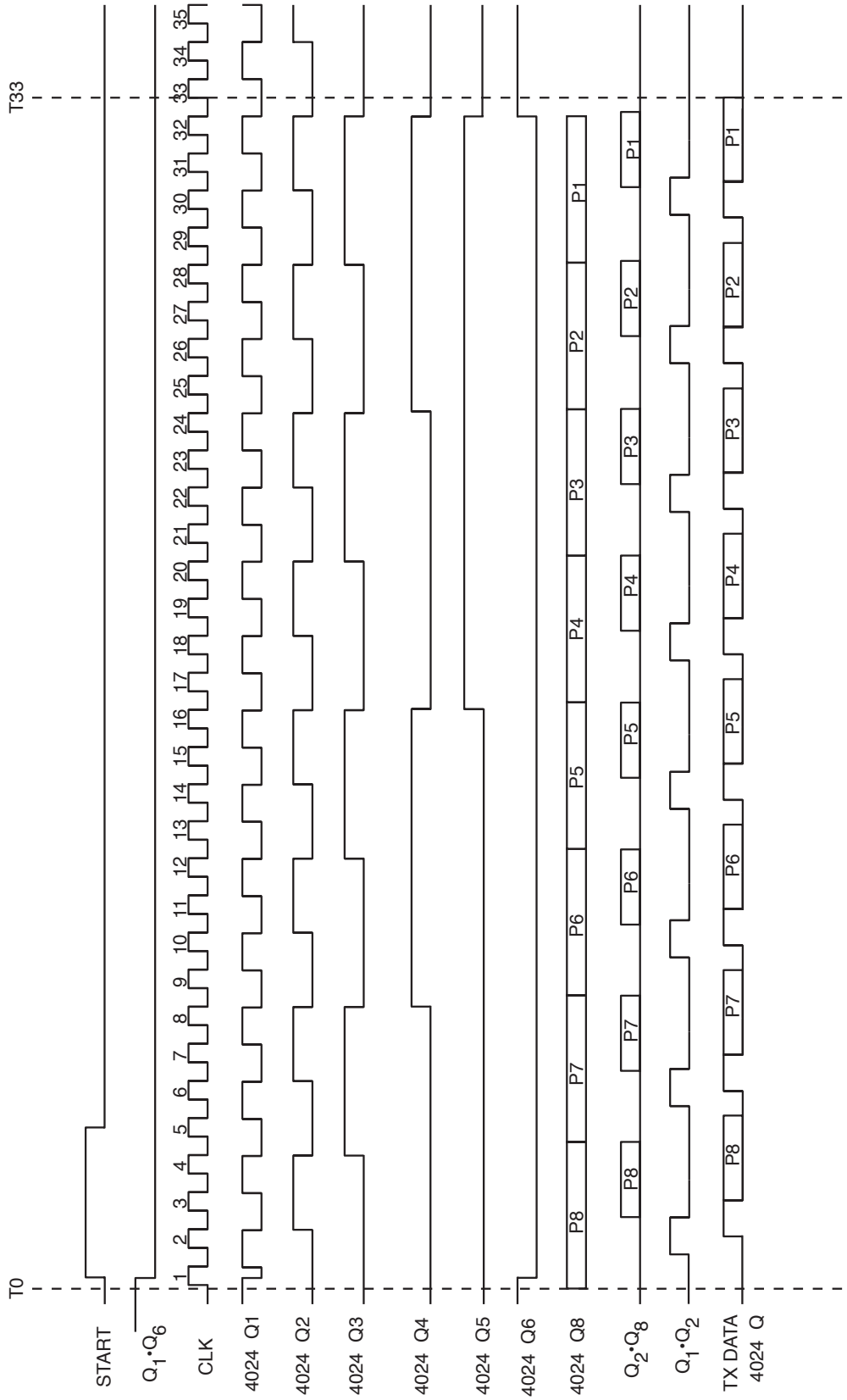


Figure 17–6. Timing Diagram — Encoder Waveforms. (1609C27)

Receiver

(The receiver is shown at the lower left of the Main Board schematic, Figure 17-27.)

The receiver (decoder) consists of I32, I38, I47, I48, I49, I50, I51, I27, I29, I43A, I45, I46, and I34. The received serial data is fed to I32 and I42 where it is clocked at 192 Hz (normal rate). The output of I42 pin 1 RECLOCKED DATA is fed to I48 pin 7, which is a dual static, 4-bit shift register. A MID-BIT CLOCK is derived from I43A and I44. (I44 is a 7-bit ripple counter that counts for a 1/2-bit period and generates a mid-bit clock to load the reclocked data into I48.) The mid-bit clock is used to sample the mid-point of the bit period to determine if there is a "1" or "0" present. The mid-bit clock is the same frequency as the incoming signal because it is derived from received data.

The parallel output from I48 are compared with data stored in I49 and I50. I49 and I50 are 4-bit magnitude comparators that compare the five (5) address bits received with the receive address, selected by switch S6 on the Auxiliary Board (see Figure 17-28, lower right). These five signals are fed to the Main Board on JMP2 pins 2, 4, 5, 9, and 3. The output of I50 pin 3, VALID ADDRESS, is fed to I32 pin 2, indicating that a valid address has been received. I27 is a DECADE counter which has an output on pin 9 after eight (8) bits have been counted, following reset. The output of I32 pin 3 signifies that eight (8) bits have been received, and that the receive address bits are correct.

The D0, D1, and H/L parallel bits that are stored in I48 are fed to I29, pins 11, 12, and 13, respectively. I29 is a QUAD-D type register that is used to store D0, D1, H/L, and VALID DATA until new data is received. The data present on I29 pins 11, 12, 13, and 14 is loaded into the register by the LATCH DATA line from I46 pin 9, which is part of the message timer. The output of I29 (pins 3, 4, 5, and 6) is fed to I51 (another 4-bit magnitude comparator). I51 compares the received data with the transmitted D0, D1, and H/ L bits. If the received bits are not the same as the transmitted D0, D1, H/L, then I51 pin 3 will be low (logic "0"), and a CHECKBACK FAIL signal will be generated on I37 pin 11. The CHECKBACK FAIL signal is fed to the Auxiliary Board on JMP1 pin 6 (see Figure 17-28, lower right).

The VALID DATA, H/L, D1, D0 signals received (see Figure 17-27, lower right) are fed from I29 to I30 solely for the purpose of generating a remote Initiate command. The last three (3) bits must be "001" to initiate a checkback sequence in the Master Checkback Module. The MESSAGE TIMER consists of I47A, I43B, I45, and I46. The first received data bit clocks through I43B and resets I45. (I45 is a seven-stage ripple counter that begins counting 192-Hz clock pulses from I47 pin 3). After 72 clock pulses (375 milliseconds), I45 (Q4, Q5, Q6, and Q7) are "1001", and I46 (a BCD-to-decimal converter) will have an output, on pin 5, which signals the end to the receive period. (The 8-bit period, with a clock of 192 Hz, is 333 milliseconds.) I46 pin 9 is used to latch the received data into I29.

(This occurs after 64 clock pulses, or 333 milliseconds.) The last "mid-bit sampling" pulse occurs after 312.5 milliseconds.

This allows all data bits to be sampled and stored before being loaded into I29.

17.8.2 Master Checkback Auxiliary Board

The Auxiliary Board contains the sequencer and sequencer programming, sequence pulse generator, checkback interval timer, and events selection circuitry.

Sequencer

(The sequencer is shown at the lower left of the Auxiliary Board schematic, Figure 17-28.)

The sequencer (I1) is a decade counter, or divider, which is used as a scanner in this application. Delay sequence clock pulses to I1 pin 14 cause sequential outputs from Q1 through Q7.

Outputs Q1 through Q6 are used when you perform the six tests (LL1, HL1, LL2, HL2, LL3, and HL3), and output Q7 is used to generate a stop command. (A stop command may also be generated by placing JU1 through JU6 in the G position—one jumper placement for each test to

be run.) This top command (at I3 pin 10) is fed to I21 pin 2 (see Figure 17-28, upper right) which generates a "stop sequencer" pulse that stops the sequence pulse generator (see "Sequence Pulse Generator" later in this chapter).

A checkback sequence is always started by the "initiate" pulse, I1 pin 15 (see Figure 17-28, lower left), which resets I1, causing Q0 to become a logic "1" and all other outputs to go low. The Q0 output (at I1 pin 3) generates the "sequence initialize" pulse, which is used to clear or reset the "checkback fail" latch, I13A (see Figure 17-28, upper right); the "events" latch, I23B via I21D (see Figure 17-28, lower right); and two latches on the Main Board, I31A and I31B (see Figure 17-27, lower right).

Following the "initiate" pulse, the "stop sequencer" pulse goes low, and the sequence pulse generator begins generating "sequence" pulses.

As the sequencer scans Q1 through Q6, "OR" gates I2 through I5 perform logic comparisons to generate D0, D1, H/L, and CBS1 to CBS6 outputs, as follows:

I2A HL1 or LL1

I2B HL3 or LL3

I2C Output for Remote 1 or 3…D0

I2D HL2 or LL2

I3A HL3 or LL3

I3B Output for Remote 2 or 3…D1

Whenever HL1, HL2, or HL3 is present, I4A produces an output. (HL is a logic "1" when selected.)

Also, D0 and D1 form a 2-digit binary code as follows:

	D0	D1
Remote 1	1	0
Remote 2	0	1
Remote 3	1	1

Table 17–3. Binary Number Generation.

	A_0	A_1	A_2	D	CBS	
LL1	1	0	0	0	0	CBS1
HL1	0	1	0	1	1	CBS2
LL2	1	1	0	0	0	CBS3
HL2	0	0	1	0	0	CBS4
LL3	1	0	1	1	1	CBS5
HL3	0	1	1	0	0	CBS6

The D0, D1, and H/L signals are fed to the Main Board (via JMP1 pins 11, 9, and 10, respectively) where they are compared against what is received to determine if there is an error (see Figure 17-28, lower left).

The CBS1 through CBS6 signals are required to store six possible tests as they are performed, so that failures can be displayed. An 8-bit addressable FAILURE LATCH (I8) is driven by gates I4B, I4C, and I5A. These gates are configured to generate a binary number for each test performed. If a test fails, the "checkback fail" line (I8 pin 3) causes the failure to be stored in the proper position in the latch. The binary number generation is illustrated in Table 17-3.

The A_1 , A_2 , and A_3 binary codes represent the six possible tests. The "D" signal shows a binary "1" when a test has failed. The "D" signal is only temporary, and is passed onto CBS lines for permanent (LED) display, on the front panel.

NOTE

The LED display on the front panel is illuminated when the test is selected; the display is cleared by a correct test response and remains illuminated if a correct test response is not received, or until it is cleared by the start of a new test, or for 5.3 seconds (depending on which option is selected).

This is accomplished by I55 and LEDs D21 through D26 (see Figure 17-28, upper right). CBS lines also generate LL Fail and HL Fail commands from I5B and I5C (see Figure 17-28, lower right).

Sequence Pulse Generator

(The sequence pulse generator is shown at the lower left of the Auxiliary Board schematic, Figure 17-28.)

The sequence pulse generator, which comprises I10D, I11D, I7, I6A, I9, and associated components, generates pulses to drive the sequencer (or scanner I1). I7 is a 7-stage ripple counter which has a 192 Hz clock at the pin 1 input. The I7/Q2 output is used to derive a 48 Hz clock. The I7/Q4 output provides 12 Hz as an input to I9, a dual-programmable BCD/binary counter.

(I9 is a "down" counter and is configured for binary.) A binary number is loaded into the counter by I6. Jumper JU8 generates binary configurations as follows:

Generates Jumper Position	Binary Divider	Pulses Per Second
A	12	1
B	24	2
C	36	3
D	48	4

The sequence pulse generator continues to run until a "stop sequencer" level is applied to I11 pin 5.

For normal operation, the 1-second waiting interval is adequate for transmission as follows:

Transmission	333 milliseconds
Receiver Responds	42 milliseconds
Remote Transmission	333 milliseconds
Total Time	708 milliseconds

The receiver message timer adds forty-two (42) milliseconds before the Remote transmitter can respond. The total time to transmit to one Remote and receive its reply is, therefore, 708 milliseconds. The only time that 2-, 3-, or 4-second waiting intervals are required would be when remotes are "daisy chained". (These times are based on a clock speed of 192 Hz.)

Sequence-Related Circuits

The following circuits affect the functions of the sequence pulse generator:

- Start transmitter pulse
- Delayed sequence pulse
- Retry on failure
- Stop at failure
- Auto initiate (normal or block on failure)
- Stop pulse generation
- Write disable

Start Transmitter Pulse

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

The "sequence" pulse (from the sequence pulse generator) is fed to I12A input "D", where it is clocked by the 48 Hz clock from the sequence pulse generator; this results in a delay of four 192 Hz clock pulses before the transmitter begins sending data. The delay allows all circuits and registers to settle before transmission begins.

Delayed Sequence Pulse

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

The "sequence" pulse (from the sequence pulse generator) is also fed to I11B and I13B, where the pulse is delayed by 2.6 milliseconds (one-half of the 192 Hz time period). The delayed "sequence" pulse is applied to I1 (see Figure 17-28, lower left), and must be delayed slightly (DELAY SEQ CLK) to avoid racing conditions.

Retry on Failure

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

This function is governed by I10A, jumper JU9, I11A, I13A, and I12B. When JU9 is placed in the YES position, the Master checkback is allowed to send the same message twice, by stopping the "delayed sequence" pulse. If a "checkback fail" command is applied to I11 pin 1, I12B will divide by two (2) and cause I10A to have a logic "1" output for every other "sequence" pulse.

Stop at Failure

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

When jumper JU11 is placed in the YES position, I21A generates a "STOP SEQUENCE" command and stops the sequence pulse generator.

Auto Initiate (Normal/Block on Failure)

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

Jumper JU14 is used to block the "auto initiate" function if a failure occurs. When JU14 is placed in the BLOCK ON FAIL position, the output from "failure" latch I13A pin 2 (Q) is fed to the Main Board and inhibits the "auto initiate" pulse.

Stop Pulse Generation

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

The stop pulse is generated by I21A, I23A, I11C, and I14. The "stop sequencer" output from I21A is used to clock a logic "1" to the output of I23A (pin 1). This allows I11C to deliver a 192 Hz clock to I14; I14 counts sixteen (16) clock inputs and resets I23A. The "stop" pulse is 83.33 milliseconds and is used to develop the LATCHED HL FAIL and LATCHED LL FAIL signals via I20A and I20B. The "stop" pulse also is used to latch the selected event into I23B (via I21B). The "stop" pulse is a different function from the "stop" command discussed previously. The "stop" pulse occurs after the "stop" command.

Write Disable

(See the upper left of the Auxiliary Board schematic, Figure 17-28.)

The "write disable" pulse is generated by I21C and 13D. This pulse (logic "1") is used to disable the "failure" latch during the time period when a "sequence" pulse, "delayed sequence" pulse, or a "stop sequencer" pulse is present to prevent data loading into the "failure" latch during switching from one test to another.

Seal-In/Momentary Alarms

(See the lower right of the Auxiliary Board schematic, Figure 17-28.)

The circuitry that determines whether the alarms are "sealed-in" or "momentary" (for 5.3 seconds) consists of I5B, I5C, I20A, I24D, I25A, I25B, I26, and jumper J12. I20A is the LL alarm latch; I20B is the HL alarm latch. Input data are fed to the latches as follows:

- LL1, LL2, and LL3 (I5B) to I20A
- HL1, HL2, and HL3 (I5C) to I20B

The "stop" pulse (previously discussed) clocks the latches to a HL or LL failure. These failures (or alarms) are stored until the next initiate pulse or for 5.3 seconds, depending on the position of JU12. As soon as the latches are set with the "stop" pulse, I26 begins counting 192 Hz clock pulses. After 1,024 clock pulses, Q10 output from I26 resets the alarm latches and also the failure latch, I18 (see Figure 17-28, lower left).

The latched HL Fail and latched LL Fail signals are fed to the Main Board on JMP1 pins 3 and 4, where they are used to energize the alarm relays.

Checkback Interval Timer

This 1- to 255-hour timer (see Figure 17-28, upper left) comprises switch S2, I15, I16, I17, I18, I19, and associated components. I15 and I16 are programmable BCD "down" counters with "N = 675" programmed into them. I15 has a BCD of "10101110", and I16 has an "0110" BCD. S7 and S8 provide a method of changing the division from 675 to another number for different clock speeds (see Figure 17-3). The preset enable PE

output from I15 and I16 occurs after 675 192 Hz clock pulses. This frequency (1.28444 Hz) is fed to I17, a 12-bit binary counter, which produces an output (at Q4) after 16 input clock pulses; another output occurs (at Q10) after 1,024 input clock pulses. Jumper JU10 allows the checkback interval timer to be operated 64 times faster than normal for module testing purposes. The normal output from I17 is one output every 3,600 seconds or (1/.284444/1024) one output per hour.

I18 and I19 are both programmable 4-bit binary "down" counters. The N binary number is loaded into the counters by switch S2. When S2 is set for one (1) hour, and jumper JU10 is in the "Faster Test" position, an initiate pulse will be generated each 3,600/64 = 56.25 seconds (rather than one pulse per hour).

Events Selection Circuitry

(See the lower right of the Auxiliary Board schematic, Figure 17-28.)

Gates I10B, I10C, I22, and I24 are used to derive nine (9) outputs from two (2) inputs: H/L and CHECKBACK FAIL. The nine (9) event outputs are attained at jumper JU13. For example:

GOOD HL TESTS	I22C pin 8 high, and I10C pin 1 low
HL FAILURES	I22A pin 1 high, and I22A pin 2 high

The other seven (7) outputs are generated in a similar manner. The event to be stored, selected by jumper JU13, is placed in latch I23B after all selected tests have been run. The "stop" pulse, generated after all tests have been performed, latches the selected event into I23B. The stored event is fed through I24D to the display circuitry. The "events" latch is reset by an "initiate" pulse or the "power-up reset" pulse.

17.8.3 Master Checkback Display Board

The Display Board (see Figure 17-28, upper right) contains the display circuitry. It is plugged-into and becomes a part of the Auxiliary Board during assembly.

The display circuitry consists of I57, I58, I52, I56, I54, QN3, DS1, and associated components. The Display Board contains six (6) LEDs for displaying the results of the six tests (LL1, LL2, LL3, HL1, HL2, and HL3), and also contains the 3-digit segment display.

The "event" pulses from the event circuitry are applied to I56D and as the clock input to I57 (pin 12). I57 is a 3-digit BCD counter that can count up to 999. This chip also contains an internal clock and a multiplexor for reading out serially the three BCD numbers stored internally. For example, if the counters had counted 347 events, the output from Q0, Q1, Q2 and Q3 would be as shown below:

BCD#	Q0	Q1	Q2	Q3
3	1	1	0	0
4	0	0	1	0
7	1	1	1	0
3	1	1	0	0
4	0	0	1	0
7	1	1	1	0

The internal clock continues scanning the three BCD numbers, so that they can be sequentially displayed on the three-digit LED display.

I56A, I56B, and I56C are used to select the particular 7-segment display for the multiplexed BCD number. I56C is the least significant bit (LSB); I56B is the most significant bit (MSB). Therefore, when the BCD (3) appears on the Q outputs, QN3 (9, 8, 10) is turned "ON" and the "3" is displayed on the MSB digit in the display. I54 and I58 are Quad analog gates that are used to remove the drive from the display when the power is "OFF".

Provision is made for the counter (I57) to maintain its internal number when power is turned "OFF". Diode D20 feeds the +5 V from the Main Board (via D19) to I57, I56, I54, I58, and I53. When the unit has power applied, the +5 V on the cathode of D20 cuts off D20 so that there is no drain on the battery.

I53A is a latch to detect overflow from I57. If the counter reaches 999 and overflows on event 1,000, an output from pin 14 sets I53A. The Q output of I53A is fed to I54 pin 11 and causes the decimal points to be illuminated in the LED display. The I53A output (Q) also prevents counting further events until the counter is reset by the events reset signal applied to I53A pin 3.

17.8.4 Remote Checkback Module

This module comprises only one circuit board, which includes: transmitter, receiver, power supply, clock oscillator, H/L keying circuits, and the "daisy-chain" inputs and outputs.

Transmitter

(The transmitter is shown at the lower left of the Remote Board schematic, Figure 17-29.)

The transmitter (encoder) consists of I1, I2, I3, I4, I5, I6, and associated circuitry. The operation of the Remote Checkback Encoder is identical to that of the Master Checkback Encoder. The timing diagram (in Figure 17-9) is the same for the Master and the Remote encoders. Switch S2 is used to set the transmit 5-bit address. The remaining three bits—D0, D1, and H/L (I6 pins 5, 6, and 7)—are either from the receive data or from I7 (X1, Y1, and Z1) if the transmission is initiated from the front panel switch (S1) or the "supervisory control initiate".

When a transmission is initiated by the Remote unit, I4A is set and I7 pins 9, 10, and 11 are logic "1". This forces the remote to send bits "001" for D0, D1, and H/ L and causes the Master to initiate a full checkback cycle. If the Remote receives an 8-bit code from the Master, the "start" command (I2 pin 9) initiates a transmission. When this occurs, I7 pins 9, 10, and 11 are low and I6 pins 5, 6, and 7 are loaded with the received data for D0, D1, and H/L, which is on I7 pins 5, 2, and 12 respectively. In other words, the Remote transmitter sends back the same D0, D1, and H/L data that it receives.

The Remote "supervisory control initiate" input is the same as for the Master and will accept 250, 125, 48 or 15 Vdc. When current is passed through D14 and the optical isolator, it effectively shorts I27 pins 4 and 5, initiating a transmission.

Receiver

(The receiver is shown at the lower left of the Remote Board schematic, Figure 17-29.)

The decoder consists of I8, I9, I10, I11, I12, I13, I14, I15, I16, I17, I18, I19, and associated circuitry. The operation is nearly the same as the Master decoder. The received data at connector pin C-6 is reclocked (I19A) and applied to shift register I9 pin 7. The MID BIT CLOCK is applied to I9 pins 1 and 9. The received data is shifted into the register and its contents examined by I10 and I11. I10 compares the first four (4) address bits, while I11 compares the fifth address bit and the D1 and D0 bits. The system receive address is loaded into I10 and I11 by switch S3, while the remote number is loaded into I11 by JU1. Jumper JU1, D11, and D12 allow "01", "10", or "11" to be loaded into pins 14 and 1 of I11. If JU1 is in position 1, the Remote will respond to LL1 or HL1 transmissions from the Master. JU1 positions 2 and 3 will respond to LL2, HL2, and LL3, HL3 transmissions, respectively. When eight (8) bits are received, and a valid address is present, I15D pin 11 gives a valid data command, and a transmitter start command is generated. When the Remote responds to the Master, the D0, D1, and H/L data are supplied by the decoder.

Power Supply

R2, I22, and I23 are used to supply +15 Vdc and +5 Vdc to the board. Most logic circuits on the Remote unit operate from +15 Vdc, while most operate from +5 Vdc in the Master. The 5-Vdc regulator supplies power for the clock oscillator (I20).

Clock Crystal Oscillator

The clock oscillator (I20) normally runs at 384 Hz, twice the frequency of the Master. JU5 normally has jumpers in A, E, and F. For other clock speeds, see Figure 17-3. JU5 was provided as a convenience for testing, to enable you to speed up the clock. Also, if system bandwidth restrictions exist, you may slow the system speed down to 128 Hz.

Power-Up Reset

This circuit (Q1, C5, and associated components) performs the same function as in the Master Checkback Module.

Daisy Chain Circuitry

(See Figure 17-28 for optional uses of daisy chain circuitry.)

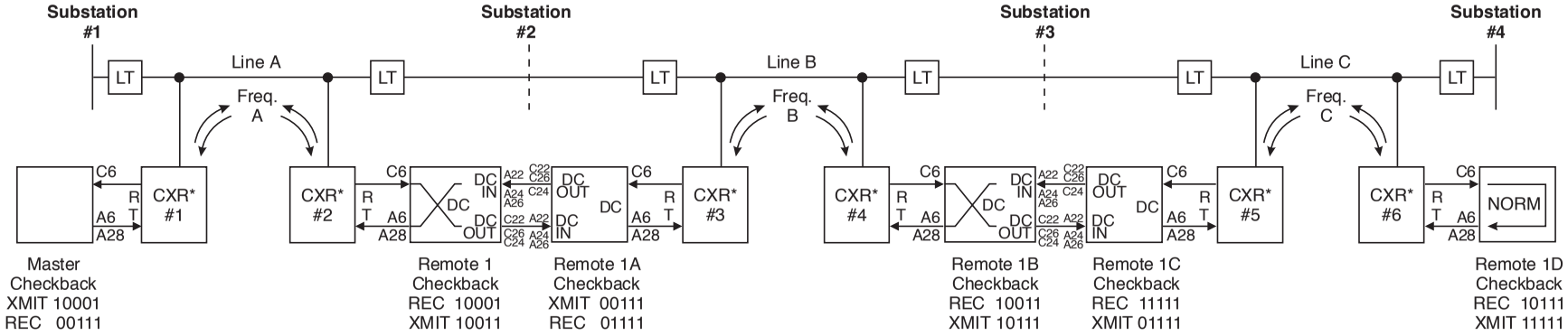
The daisy chain circuitry is provided to allow serial operation of several Remote Checkback Modules (see Figure 17-1). When JU2 is in the normal position, the HL and LL TX data is routed to QN1 (5, 6, and 7) and QN1 (1, 2, and 3) for 1 W or 10 W keying. When JU2 is placed in the daisy chain position (B), the daisy chain input (connector pins A-22, A-24, and A-26) is routed through Q2 and Q3 and keys the transmitter to 1 W or 10 W. The received data that is retransmitted (HL/LL TX DATA) is routed to the daisy chain output (connector pins C-22, C-26, and C-24). Figure 17-7 illustrates a daisy chain arrangement using one Master and five Remotes.

The Master carrier transmits address “10001”, which is received (on frequency “A”) by Remote R1; Remote R1 retransmits code “10011”. The HL/LL TX DATA from Remote R1 is daisy-chained to outputs C-22, C-26, and C-24, and is fed to Remote R1A daisy chain inputs A-22, A-24, and A-26. Carrier #3 transmitter is keyed with transmit code “10011”. This is the receive code for Remote R1B. (Carriers #3 and #4 can operate on a different frequency as compared to Carriers #1 and #2.)

Remote R1B responds to receive code “10011”, and retransmits address “10111”. This HL/LL TX DATA is daisy-chained from connector pins C-22, C-26, and C-24 on Remote R1B to connector pins A-22, A-24, and A-26 on Remote R1C. Carrier #5 transmitter is keyed with the transmit address “10111”. This completes the transmit path from Master to Remote.

Remote R1D responds to address “10111” and retransmits, via Carrier #6, the transmit address “11111”. Carrier #5 receives the signal from Carrier #6 and feeds it to Remote R1C. Remote R1C responds to receive address “11111” and retransmits the transmit code “01111” to Remote R1A. Remote R1A retransmits address “00111” back to the Master to complete the daisy-chain cycle.

All five Remotes (1, 1A, 1B, 1C, and 1D) must have JU1 (Remote number) set to the same Remote number, because these two bits are generated by the Master. ***The INITIATE push-buttons on the Remotes will not generate a full checkback cycle from the Master because the “001” code will not be recognized by the other Remotes in the daisy chain.***



* CXR (Carrier Transmitter – Receiver)

Figure 17–7. Daisy-Chain Operation through Three Substations. (1609C29)

17.9 Checkback Troubleshooting

Test Equipment

You will use the following equipment when performing tests of the TC–10B Automatic Checkback System:

- Storage Oscilloscope (TEKTRONIX 7623A)
- VOM (Simpson 270)
- Counter (HP 5381A)
- Synthesizer (HP 3325A)
- IC Clip (AP IC16 — 5 required)
- Checkback Test Fixture (must be constructed)
- Cables for JMP1 and JMP2 (used only for troubleshooting the Auxiliary Board, these cables must be constructed)

Overview

The tests in 17.9.1 and 17.9.2 are general tests to determine the overall performance of Master and Remote checkback units, using the connections shown in Figure 17-8.

The tests in 17.9.3 are more detailed and allow you to troubleshoot individual circuit blocks. They do, however, require the construction of a test fixture, as shown in Figure 17-26, as well as jumper cables (JMP1 and JMP2).

NOTE

For troubleshooting, you can shift the Auxiliary Board to the side and connect it to the Main Board with ribbon cables. These cables (for JMP1 and JMP2) are required only when troubleshooting the Auxiliary Board. They connect between the Main Board (see Figure 17-10) and the Auxiliary Board (see Figure 17-11) using the connector hardware specified in the parts list (later in this chapter).

17.9.1 Master Checkback Module (General Operation)

The Master Checkback Module comprises three PC Boards: Main, Auxiliary, and Display. You can check the Master Main PC Board (see Figure 17-10) by applying primary power (connector pins A-2/A-4 +20 Vdc, pins A-30/A-32, C-30/C-32 negative). You can place jumper JU10 on the Auxiliary Board (see Figure 17-11) in the A position and generate an "auto initiate" pulse every 56.25 seconds.

Place switch S2 on the Auxiliary Board in the one-hour position (see Figure 17-28). A more practical approach is to apply a faster frequency to the "supervisory control" input (connector pins C-8 and C-10). Because the 8-bit word is 333 milliseconds, a 1 Hz frequency applied to the supervisory control will generate an 8-bit word each second, and you can more easily observe the output on an oscilloscope (56.25 seconds and 333 milliseconds are based on the clock frequency of 192 Hz). If a signal source (1 Hz) is not available, you can place JU8 in the A position (1.5 seconds) and remove D6. I1 will continually scan with one 8-bit sequence every 1.5 seconds. No jumper can be placed in the G position, or the scan will stop. You can configure jumpers JU1 through JU6 to transmit all combinations of tests you want to perform. You can "OR" gate HL/LL TX DATA together from connector pins A-6 and A-28.

Figure 17-9 (upper and lower) shows two pictures of the actual transmitted data. There are two traces in the upper figure. The top trace is a transmitted word. The transmitted word has an address code of "10101". The last three bits are "101". The "101" code is D0, D1, and H/L and represents HL1. The bottom trace is the same 8-bit word after passing through the transmitter and the receiver. The lower figure has only one trace; it has an address of "10101," and the last three (3) bits ("100") represent LL1.

For troubleshooting, you can shift the Auxiliary Board to the side and connect it to the Main Board with ribbon cables. You must provide a cable for JMP1 and JMP2. You can use a serial shift register to provide enough time delay and merely feed the

transmitter output through the shift register and back into the receiver input. Figure 17-8 illustrates two methods of checking the checkback encoder and decoder operation. (Figure 17-12 shows the Master Display Sub PC Board.)

17.9.2 Remote Checkback Module (General Operation)

Although the Remote Checkback Module circuits are not equivalent to the Master Checkback Module circuits, all of the procedures above apply to the Remote Checkback Module. (Figure 17-13 shows the Remote PC Board.)

17.9.3 Detailed Circuit Analysis Using Test Fixture

Test Fixture Setup

You test the TC–10B Checkback Modules using the TC–10B Checkback Test Fixture (see Figure 17-26), which is designed to test both the Master and the Remote Checkback Modules. Connect connector J1 to the board you are testing.

> NOTE
>
> If the checkback test fixture is not available, you may test the Master and Remote Checkback Modules back-to-back (as shown in Figure 17-8). If two TC–10B units are available, you may test the checkback by connecting the TC–10Bs back-to-back through a 2- to 40 dB attenuator. (See "Optional Checkback System Tests" in Chapter 5, Acceptance Tests.)

When testing the Master Checkback Module using the test fixture, connect the Auxiliary Board to the Main Board with ribbon cables (construct these cables for JMP1 and JMP2). This allows you to view nearly all circuits for testing. You can lay the board flat on the bench or support it in a bench-type PC board holder. Provision is made in the test fixture for testing a Remote with a Master. Connectors J2 through J6 allow you to test one Master with up to five Remotes for Daisy-Chain operation.

You can use test fixture component J7 (BNC) for automatically cycling the checkback to initiate sequence pulses which shorten testing time. Setting the Synthesizer to 0.25 Hz will generate an initiate pulse every four (4) seconds. This is adequate time for the Master to transmit, and the Remote to receive and transmit back.

Use test fixture components S1, TP1, and TP2 to measure the current drawn by the modules you are testing.

Use test fixture component S2 to feed the daisy chain output back to the daisy chain input for testing Remotes.

Use TP3 to monitor both HL and LL transmit data from the unit you are testing.

You can use TP4 to monitor the receive data coming back into the unit you are testing.

You can plug a shift register board into J2 to generate a sufficient time delay for checking receive operation on the unit you are testing.

You should normally use a Remote unit as part of the test, if one is available.

Master Checkback Testing

To test the Master Checkback Module, complete the following 17 steps.

1. Preliminary Setup

   Make sure that switches S1, S3, and S4 are all "OFF". Check jumpers JU1 through JU7 to make sure that only one jumper is in the G position and that no two jumpers are in the same position. Turn S1 "OFF" and plug in the board to J1.

> **⚠ CAUTION**
>
> **ALWAYS TURN S1 "OFF" BEFORE REMOVING OR INSERTING CHIPS OR CHANGING JUMPERS ON THE BOARD.**

   Connect the VOM between TP1 (Negative) and TP2 (Positive) and monitor the input current to the module. The initial input current

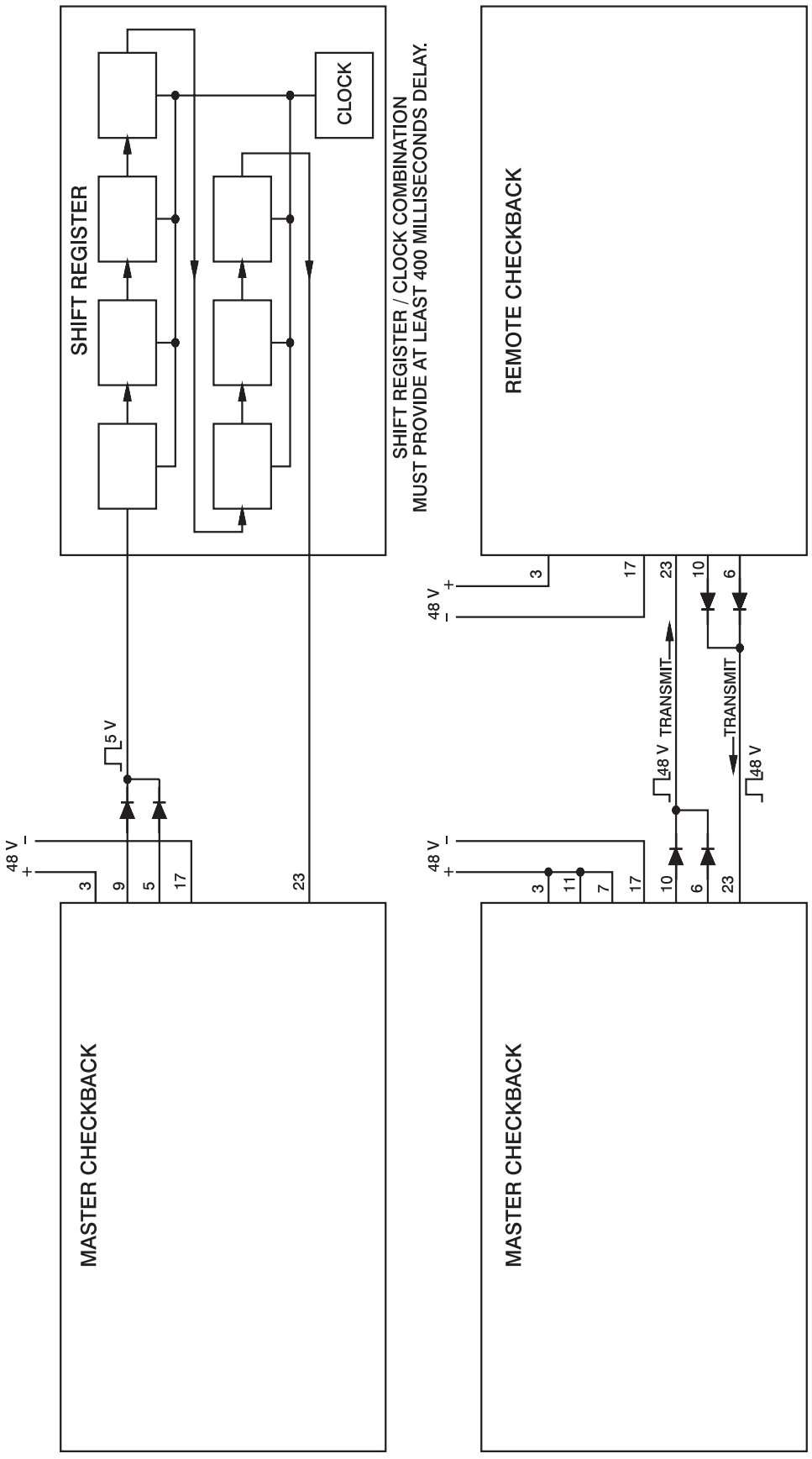
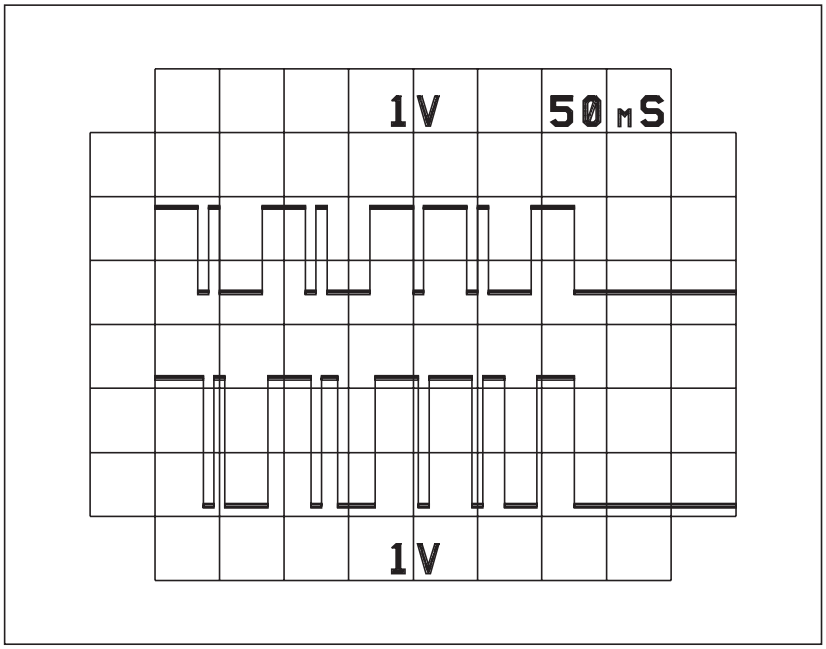


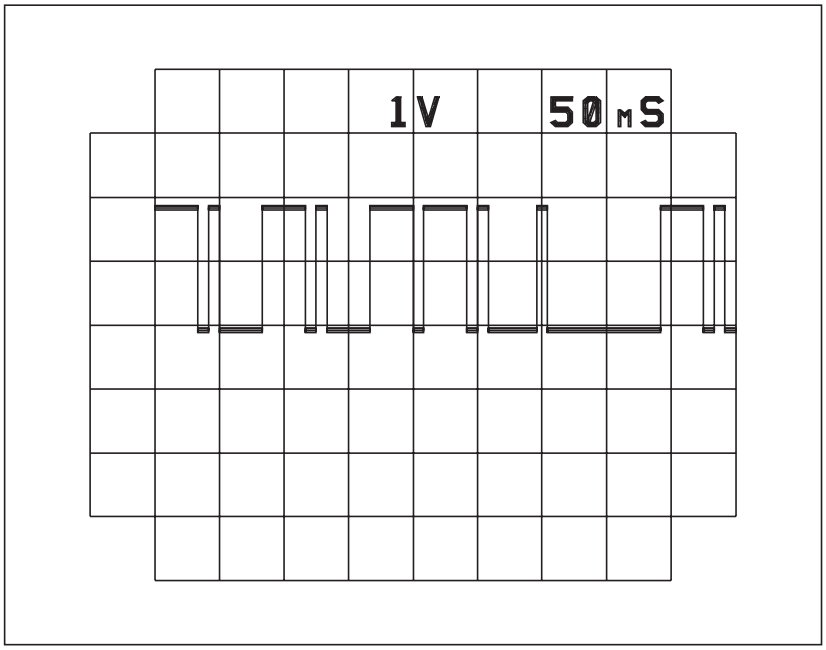
Figure 17–8. Troubleshooting Checkback Encoder/Decoder Operation. (1607C99)



Top Trace

Bottom Trace

Upper Figure



Lower Figure

Figure 17–9. Timing Diagram — Transmitted Waveforms. (9647A76)

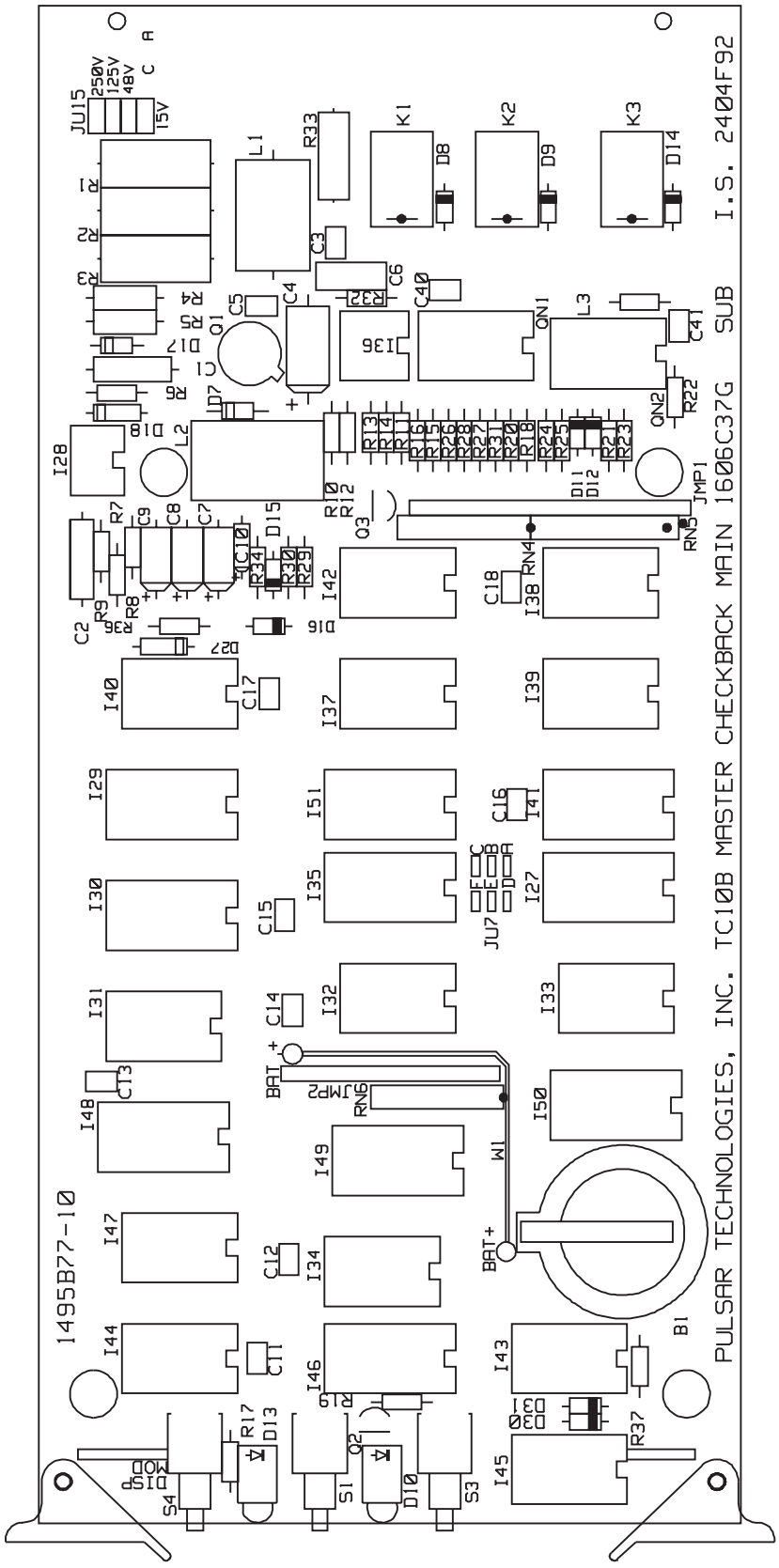


Figure 17–10. Automatic Checkback PC Boards — Master Main Board. (1495B77)

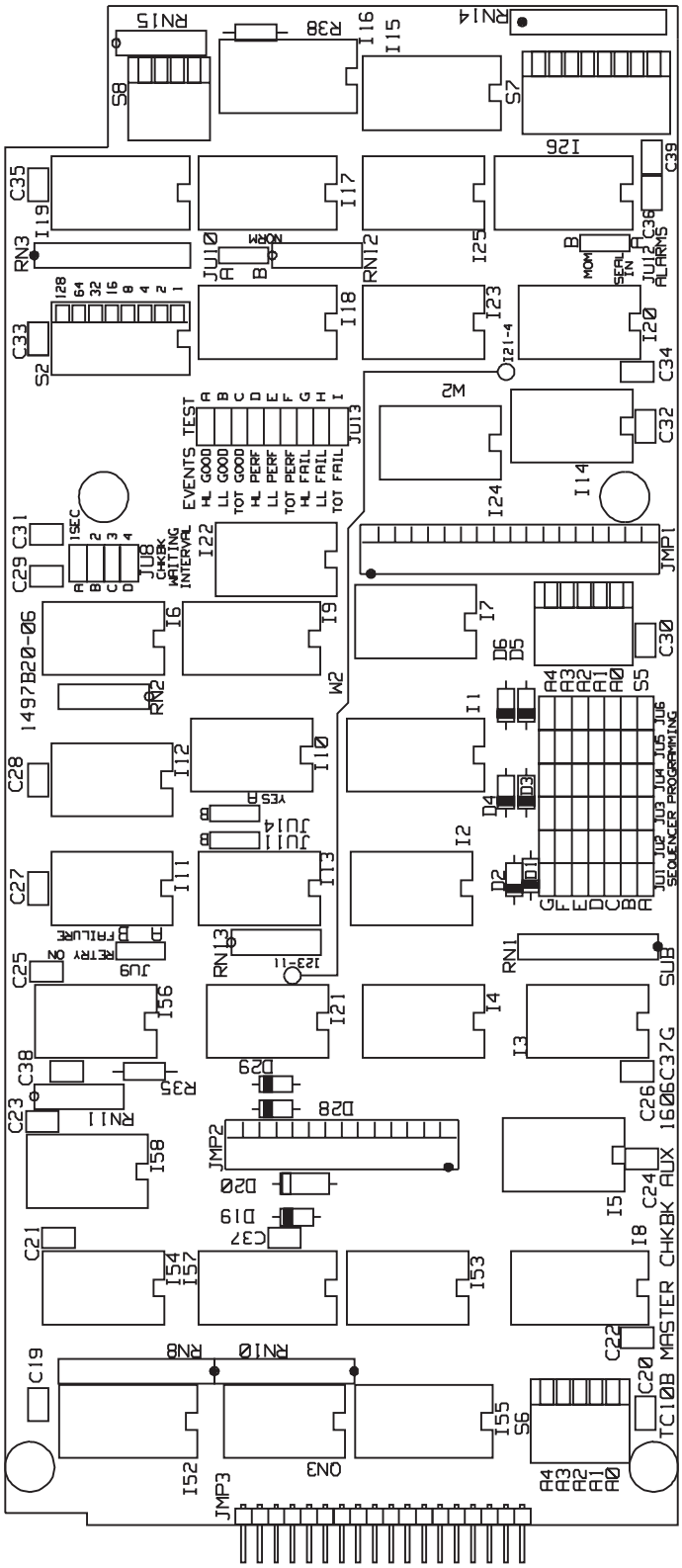


Figure 17–11. Automatic Checkback PC Boards — Master Auxiliary Board. (1497B20)

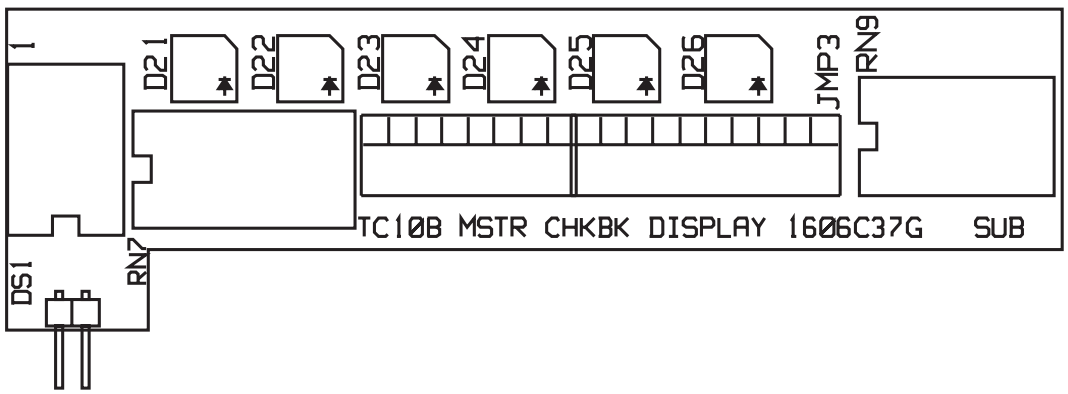


Figure 17–12. Automatic Checkback PC Boards — Master Display Sub Board. (9648A08)

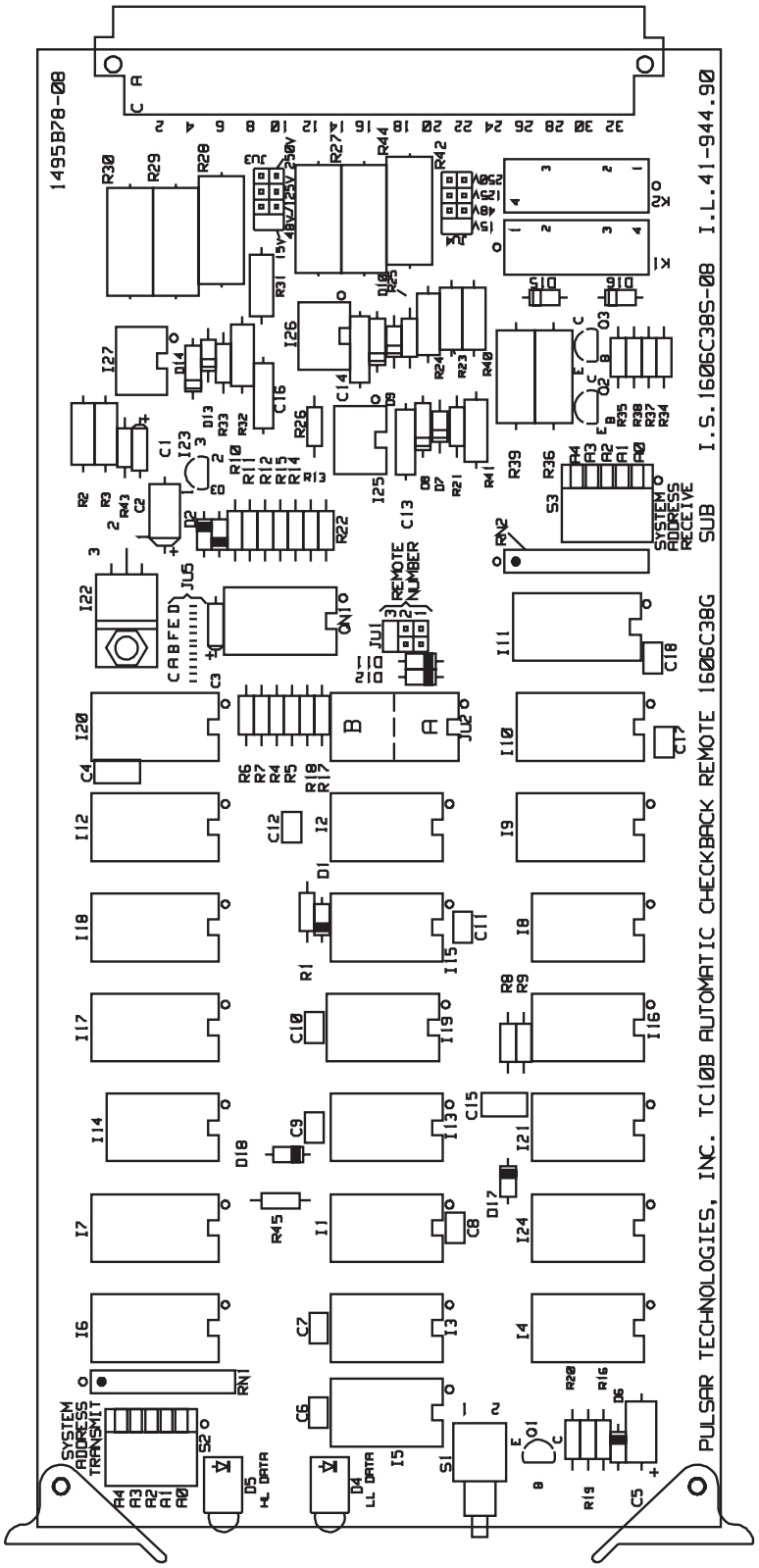


Figure 17–13. Automatic Checkback PC Boards. — Remote Board. (1495B78)

should be approximately 48 mA and should fall to less than 15.3 mA, except when the counter counts an error. Higher currents than 48 mA indicate a bad chip or a chip with a pin not in the socket. Remove the VOM.

On the Main Board, check timer jumpers JU7A, JU7B, and JU7C.

For a desirable clock frequency of 192 Hz, you must set JU7A.

2. Check for five (5) Volts (Main Board).

   With S1 "ON", check between the ground (common) and cathode of D8 for +5 V ±5% (see Figure 17-27, upper right).

3. Power-Up Reset (Main Board)

   With the oscilloscope, monitor between the ground (TP5 on the test fixture) and the collector of Q3 (see Figure 17-27, upper left). Turn S1 "ON" and note that Q3 collector goes high (+5 V) for one (1) to five (5) seconds. Turn S1 "OFF".

4. Clock Oscillator (Main Board)

   Monitor pin 9 of I35 with a counter and an oscilloscope (see Figure 17-27, lower right). Turn S1 "ON". The clock frequency should be 1,000 times faster than 192 Hz (i.e., 192 kHz) for the duration of the "power-up reset" pulse and should settle down to 192 Hz after the "power-up reset" has fallen to zero (0) volts.

5. Sequence Pulse Generator and Sequence Circuitry (Auxiliary Board)

   Place a jumper from I3C pin 10 to I3B pin 7 (Gnd). This will disable the "stop" command. Place jumpers as follows: JU1-A, JU2-B, JU3-C, JU4-D, JU5-E, JU6-F. The sequence pulse generator should generate a "sequence" pulse every 1.0 seconds with JU8 in position A. Monitor the "sequence" pulse with the oscilloscope on I9 pin 1. It should be 166 milliseconds. The sequence circuit (I1, JU1 through JU7) should scan Q0 through Q9 outputs and should cause the LEDs on the Auxiliary board to light sequentially for LL1, HL1, LL2, HL2, LL3, and HL3 for each "sequence" pulse.

   Note that there will be four "sequence" pulses that will cause an LL LED to come "ON". This is caused by I1 on the Main board counting Q7, Q8, Q9, and Q0.

6. HL/LL Transmit Data

   Using the same setup as in Step 5 (above), note that LL Data and HL Data LEDs on the Main Board are coming "ON" in sequence with the LEDs on the Auxiliary Board. Use the oscilloscope to monitor TP3 (on the test fixture) to see if QN2 (9, 10, 8) and QN2 (12, 13, 14) are switching 10 to 20 V pulses to the system output.

7. Transmit Address

   Monitor TP3 with the oscilloscope and adjust the sweep speed to 50 milliseconds per division. Adjust the oscilloscope to store and note the bit lengths. A "1" should be 31.25 milliseconds; a "0" should be 10.42 milliseconds. The first five (5) bits transmitted are the address bits; the last three (3) bits are data bits. Check the address bits by setting S5 (on the Auxiliary board) to all "0" (all switches up). Then, one at a time, set A0 to "1", A1 to "1", A2 to "1", until the transmitted address code is all "1". Check the oscilloscope for the proper response. The last three bits can also be checked. The final bit is H/L and is a "1" for High-Level; a "0" for Low-Level. As the sequence is scanned, the last bit will alternate from "0" to "1" in sequence with the LED indicators. The following table illustrates a sequence as observed on the scope.

	LAST 3 BITS		
LL1	1	0	0
HL1	1	0	1
LL2	0	1	0
HL2	0	1	1
LL3	1	1	0
HL3	1	1	1
Q7	0	0	0
Q8	0	0	0
Q9	0	0	0
Q0	0	0	0

8. Initiate Circuitry (Auxiliary Board)

   Remove the jumper connecting I3B pin 7 to I3C pin 10.

   Arrange jumpers JU1 through JU7, as follows: JU1-A, JU2-B, JU3-G, JU4-D, JU5-E, and JU6-F. Press the manual INITIATE button (S3) on the front panel. LL1 and HL1 should be transmitted. Place JU15 in the 15 V position.

   a) Supervisory Control Initiate

      Connect the synthesizer to J7 on the test fixture.

      Adjust the synthesizer as follows: .25 Hz, 8.5 V p-p (square wave output). LL1 and HL1 should be generated every four (4) seconds. Remove the synthesizer from J7 of the test fixture.

   b) Auto Initiate

      Connect jumper JU10 to position A, and move the SW1 position of S2 to the down position. This configuration will generate an "initiate" pulse every 56.25 seconds. Each "initiate" pulse should generate an LL1 and an HL1. If the center pin of JU10 is connected to I17 pin 9, an "initiate" pulse will be generated every seven (7) seconds.

9. Checkback Interval Timer (Main Board)

   The Checkback Interval Timer is normally supposed to deliver an "initiate" pulse from 1 to 255 hours. The clock frequency of 192 Hz is impractical for testing.

   To speed-up the frequency to 192 kHz (1,000 times faster), jumper +5 V through a 1 K resistor to pin 10 of the I35 clock oscillator. The checkback interval timer will then be programmable (with JU10 in the A position) from one pulse every 56.25 milliseconds to one pulse every 14.34 seconds. Monitor I18, pin 3 (on the Auxiliary board) with the oscilloscope and adjust S2, using SW1, SW2, SW3, SW4, SW5, SW6, SW7, and SW8. Note that the 56.25-millisecond interval doubles each time a switch is set, so that position SW8 should produce 7.2 seconds. Close all switches of S2 (SW1 through SW8), and the time should be 14.34 seconds. Press the front panel (checkback interval) TIMER RESET switch (S1) and note that all counters (I5, I6, I7, and I8) are reset. If you move the switch (S1) down and up, it should be 14.3 seconds before the first "initiate" pulse occurs.

   Restore the clock to 192 Hz.

> **NOTE**
>
> Now test the Master Checkback Module with a Remote Module or the shift register card.

10. Check (Optional) Events Counter (Auxiliary Board)

    If the Events Counter is part of the system, you should set the checkback interval counter to JU10-B; you should set S2 to all ones. Connect the external synthesizer/generator unit to J7 on the test fixture.

    Set the synthesizer to 0.25 Hz and 8.5 V p-p (square wave output). This will generate a LL1/ HL1 every four (4) seconds.

    With the Master recording no errors, set jumper JU13 to position A; the counter should count all good HL tests.

Set jumper JU13 to position B; the counter should record all good LL tests.

Set jumper JU13 to position C; the counter should record all good LL and HL tests.

Set jumper JU13 to position D; the counter should record all the HL tests performed.

Set jumper JU13 to position E; the counter should record all LL tests performed.

Set jumper JU13 to position F; the counter should record the total of all tests performed.

Set jumper JU13 to position G; the counter should record all HL failures.

> NOTE
>
> Failures are caused by changing an address.

Set jumper JU13 to position H; the counter should record all LL failures.

Set jumper JU13 to position I; the counter should record all failures.

11. Re-Try (Auxiliary Board)

    With jumper JU9 in position B, the Master will send each test twice. Change an address to create an error and note that LL1 is sent twice, and HL1 is sent twice. Monitor the output wave shape with the oscilloscope.

12. Stop at Failure (Auxiliary Board)

    With jumper JU11 in the A position, create an error in LL1; note that only LL1 is transmitted when the sequence circuit is set to send LL1 and HL1.

13. Seal-In/Momentary Alarms (Auxiliary Board)

    With jumper JU12 in the B position (5.3 seconds), the alarm lights should remain on for 5.3 seconds. (Slow down the synthesizer to .1 Hz for 10 seconds.) Set JU12 at position A, and the alarms will remain "ON" until the next initiate pulse occurs.

14. Auto Initiate (Auxiliary Board)

    With the Auto Initiate Timer set for 56.25 seconds (as in Step 9, above), set jumper JU14 at the A position. The first auto initiate pulse will operate LL1 and HL1. All subsequent pulses should be blocked (after the failure of LL1 or HL1).

15. Check HL and LL Alarm Relays (Main Board)

    With the Master recording HL and LL alarms, turn test fixture S4 "ON". With the oscilloscope, check connector pin C-14 (for normally-closed) and connector pin C-18 (for normally-open) for HL alarms (see Figure 17-27, upper right). In a similar manner, check pins C-22 (for normally-closed) and C-26 (for normally-open) for LL alarms. Turn test fixture S4 "OFF".

16. Events Relay (Main Board)

    With the Events Counter counting, turn on test fixture S3. Monitor connector pins A-22 and A-26 to see if 20 volts is being switched by relay K3 when the Events Counter counts. Turn "OFF" test fixture S3.

17. Receive Addresses (Auxiliary Board)

    On the Auxiliary Board, check all combinations of receive addresses by placing 5-position dip switch S6 in the all zeros position (all switches up). If using the shift register, change the related transmit switches (S5) to all zeros. If you are using a Remote, change the transmit switch on the Remote. Go from all zeros to all ones for A0, A1, etc., one-at-a-time until all switches have changed from zero to one. This concludes the test for the Master Checkback Module.

Remote Checkback Testing

To test the Remote Checkback Module, complete the following 10 steps.

1. Preliminary Setup

   Plug the Remote Board into the J1 test fixture. Monitor between TP1 and TP2 with the current meter. The current should read 33 to 40 mA. Excessive current indicates a bad chip on the board or a chip with an open pin. If the current is okay, remove the VOM from TP1 and TP2 and turn S1 "ON". On the Remote Board, set all the A positions at jumper JU2 for normal operation.

2. Power Supply

   At the test fixture, measure the voltage between TP5 pin 17 and I22 pin 1 (see Figure 17-29, upper right). The voltage should be 18 to 20 Vdc. Check I22 pin 3 for 15 Vdc ±5%. Check I23 pin 1 for 5 Vdc ±5%.

3. Clock Oscillator

   Monitor I20 at pin 9 with a counter and an oscilloscope. With a jumper at JU5 position A, the frequency should be 384 Hz. Change JU5 jumper to position B; the frequency should be 192 Hz. With jumpers in both positions (A and B) of JU5, the frequency should be 128 Hz. With a jumper at JU5 position A, measure the frequency of I21 pin 1; it should be 192 Hz (after dividing down from 384 Hz). Similarly, the frequency of I21 pin 12 should be 96 Hz.

4. Power-Up Reset

   Turn "OFF" test fixture S1. Turn S1 "ON" and monitor the collector of Q1, as it goes to 15 volts for 1 to 5 seconds.

5. Initiate Circuit

   Monitor test fixture TP3 with the oscilloscope. Adjust the oscilloscope to 50 milliseconds per division (in store mode). On the Remote front panel, depress S1; a sequence of pulses should appear. If the initiate operates, connect the external synthesizer/generator unit to test fixture J7. Set the synthesizer to 0.25 Hz and 8.5 Vp-p (square wave output). Connect JU3 to the 15-V position.

   Every four (4) seconds, an "initiate" pulse should be generated and a code transmitted. On the test fixture, check the waveform at TP3 for 10 to 18 Vdc output at HL and LL.

6. Transmit Address

   Set Remote switch S2 to all zeros (all switches up).

   The first five bits transmitted should be all zeros (10.42 milliseconds). Close S2-1 (A0/) through S2-5 (A4) and note that the first five bits all become "1".

   Check the last 3 bits; they should be "001".

> **NOTE**
>
> This code is recognized only by the Master Checkback Module, not by the Remote Checkback Module.

7. HL DATA Send LED

   On the Remote front panel, check the "HL DATA" LED to see if it flashes in sequence with data being transmitted.

> **NOTE**
>
> The "LL DATA" LED only comes "on" when LL data is transmitted by the Master Module.

8. Daisy Chain Circuits

   On the Remote Module, set all "B" jumpers at JU2 for daisy chain operation. Place JU4 in the 15 V position. At the test fixture, turn "ON" switch S2. This connects the daisy chain output to the daisy chain input. HL data should be on connector pin C-22. LL data should be on connector pin C-24 (see daisy chain positions 1 through 4). Move the oscilloscope to test fixture TP3 (connector pins A-6 and A-28). The HL/LL transmit data should be the same as on connector pins C-22 and C-24.

9. Receiver (Decoder)

   This test must be performed with a Master Checkback Module, because the "001" code transmitted by the Remote will not be recognized by another Remote.

> NOTE
>
> The shift register time delay cannot be used.

   With the Master plugged into the test fixture at J2 and scanning LL1, HL1, LL2, HL2, LL3, and HL3, (with no jumpers in position G of Master Module jumpers JU1 through JU6, and with a jumper from I3C pin 10 to I3A pin 7), set jumper JU1 to position 1; the Remote should recognize LL1 and HL1 and transmit a code back to the Master.

   Set jumper JU1 to position 2; the Remote should recognize LL2 and HL2 and respond to the Master.

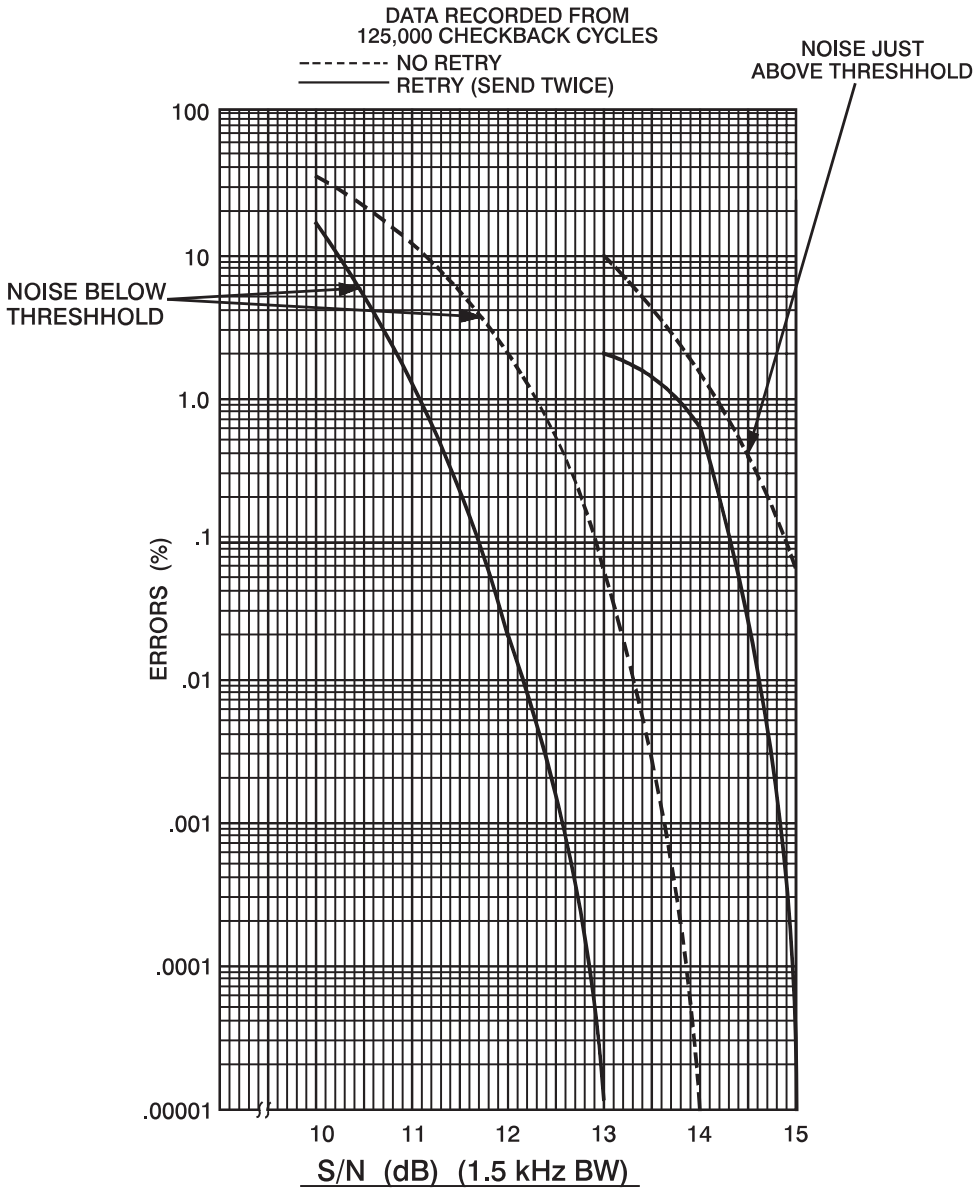
   Set jumper JU1 to position 3; the Remote should recognize LL3 and HL3 and respond to the Master.

10. Receiver Address

    Check all possible combinations of receiver address by placing S3 (on the Remote) in the all "0" position. On the Master, change the transmit address to all zeros. Then, progressively, make A0, A1, A2, A3 and A4 addresses all "1".

Daisy Chain Testing

The test fixture can accept up to five (5) Remotes for testing daisy chain operation. The daisy chain schematic (see Figure 17-7) illustrates the sequence of the addresses which are used, so that data signals can pass from the Master through the daisy chain and back to the Master.



NOISE TEST CONDUCTED ON THE DIGITAL CHECKBACK RESULTED IN THE PLOT OF % ERRORS Vs S/N (dB) IN A 1.5 kHz BANDWIDTH. THE SIGNAL TO NOISE RATIO WAS MEASURED AT THE RECEIVER 20 kHz IF. TESTS WERE CONDUCTED WITH SIGNAL TO NOISE RATIOS OF 10 dB TO 15 dB USING NO RETRY AND RETRY. IT CAN BE SEEN THAT WHEN THE CHECKBACK IS CONFIGURED TO SEND TWICE, THE ERROR RATE IS GREATLY IMPROVED. INTERMITTENT FAILURES OF THE CHECKBACK MAY BE DUE TO THE S/N AT THE RECEIVER LOCATION AT THE TIME THE CHECKBACK OCCURS. THIS MAY BE AN INDICATION THAT THE RECEIVER IS OPERATING BELOW THE RECOMMENDED 20 dB S/N FOR A BLOCKING RELAY SYSTEM.

Figure 17–14. Digital Checkback Signal/Noise Data. (1609C86)

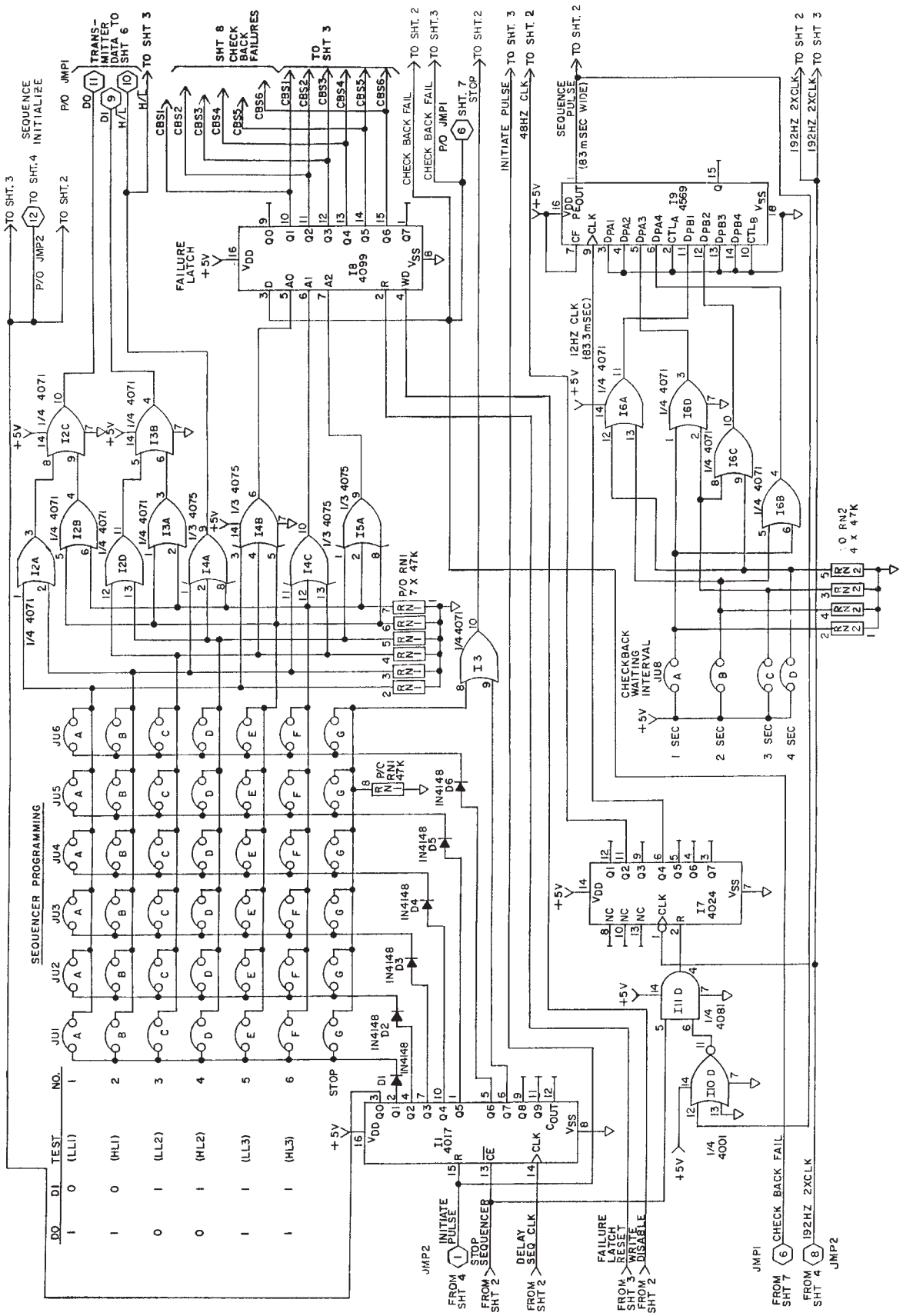


Figure 17–15. Master Checkback Schematic — Auxiliary Board. (1606C37, Sheet 1)

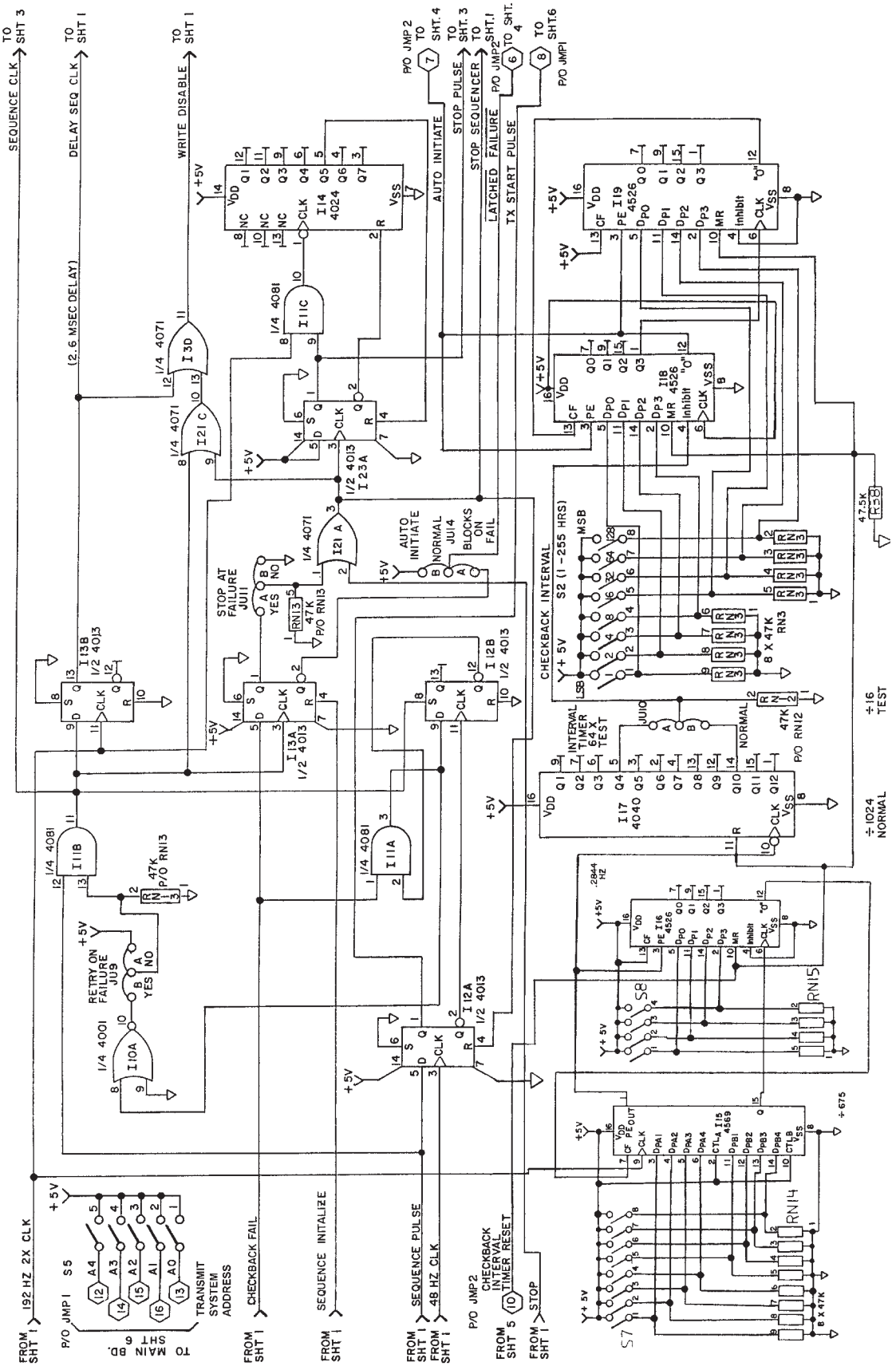


Figure 17–16. Master Checkback Schematic — Auxiliary Board. (1606C37, Sheet 2)

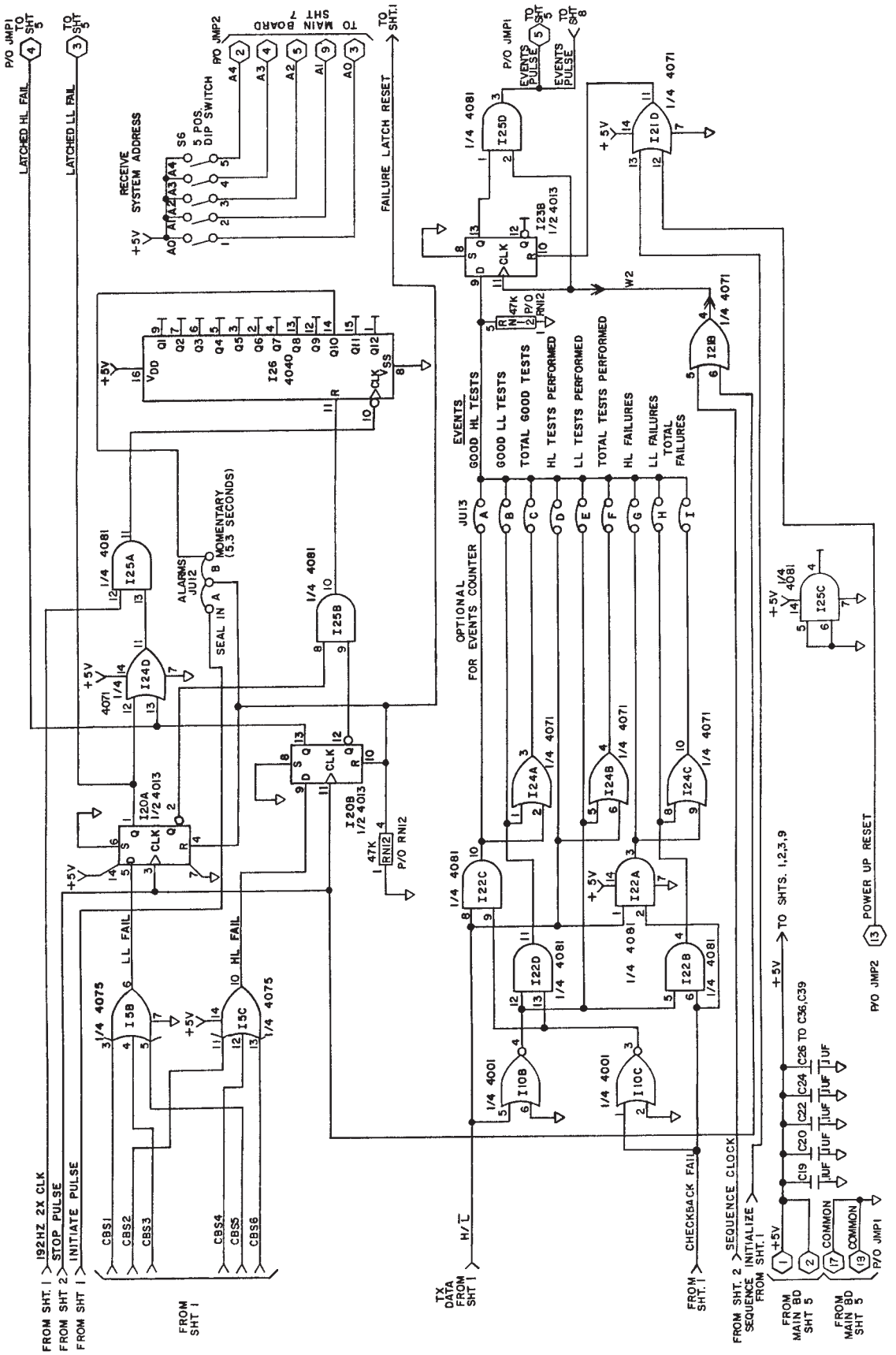


Figure 17–17. Master Checkback Schematic — Auxiliary Board. (1606C37, Sheet 3)

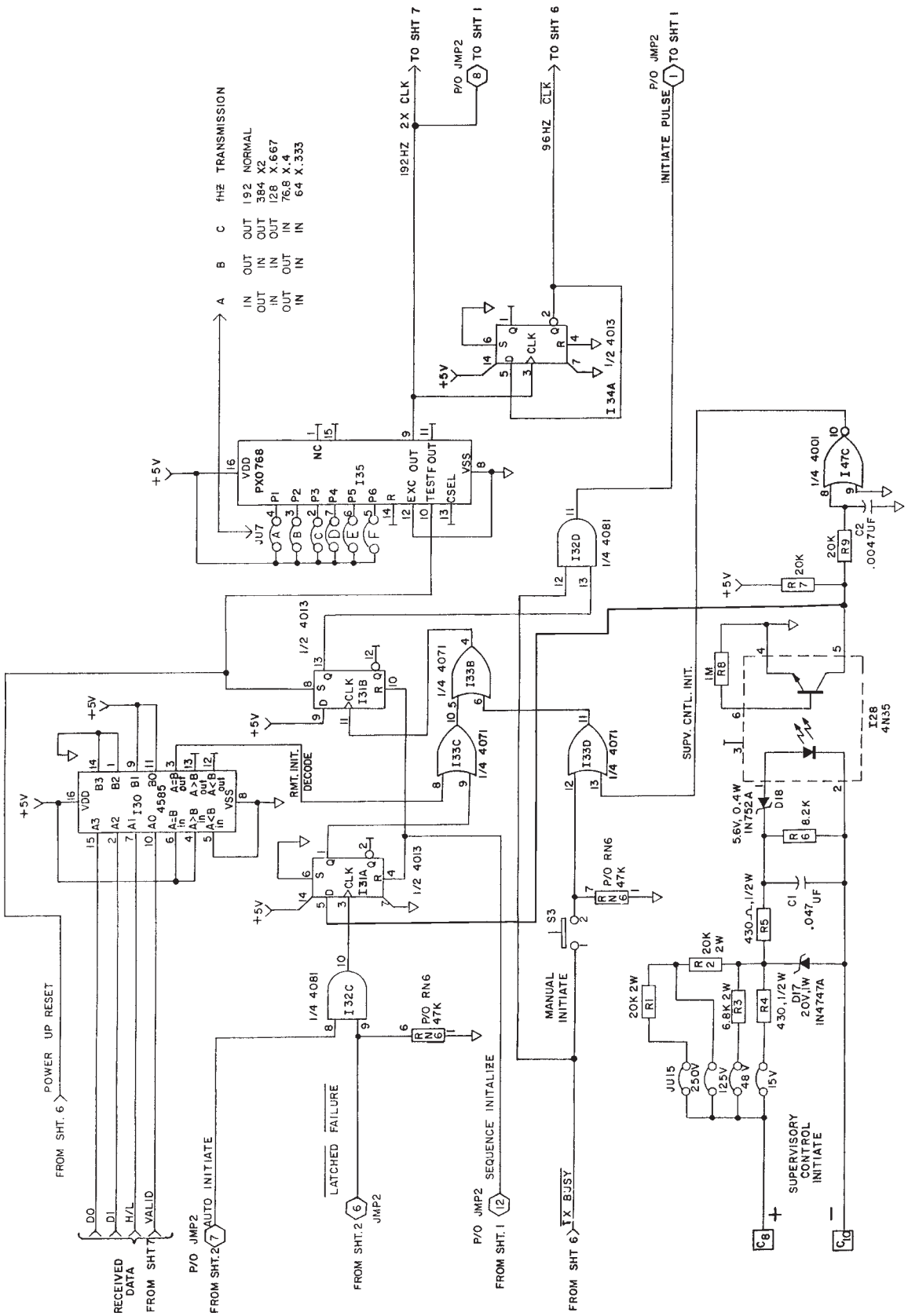


Figure 17–18. Master Checkback Schematic — Main Board. (1606C37, Sheet 4)

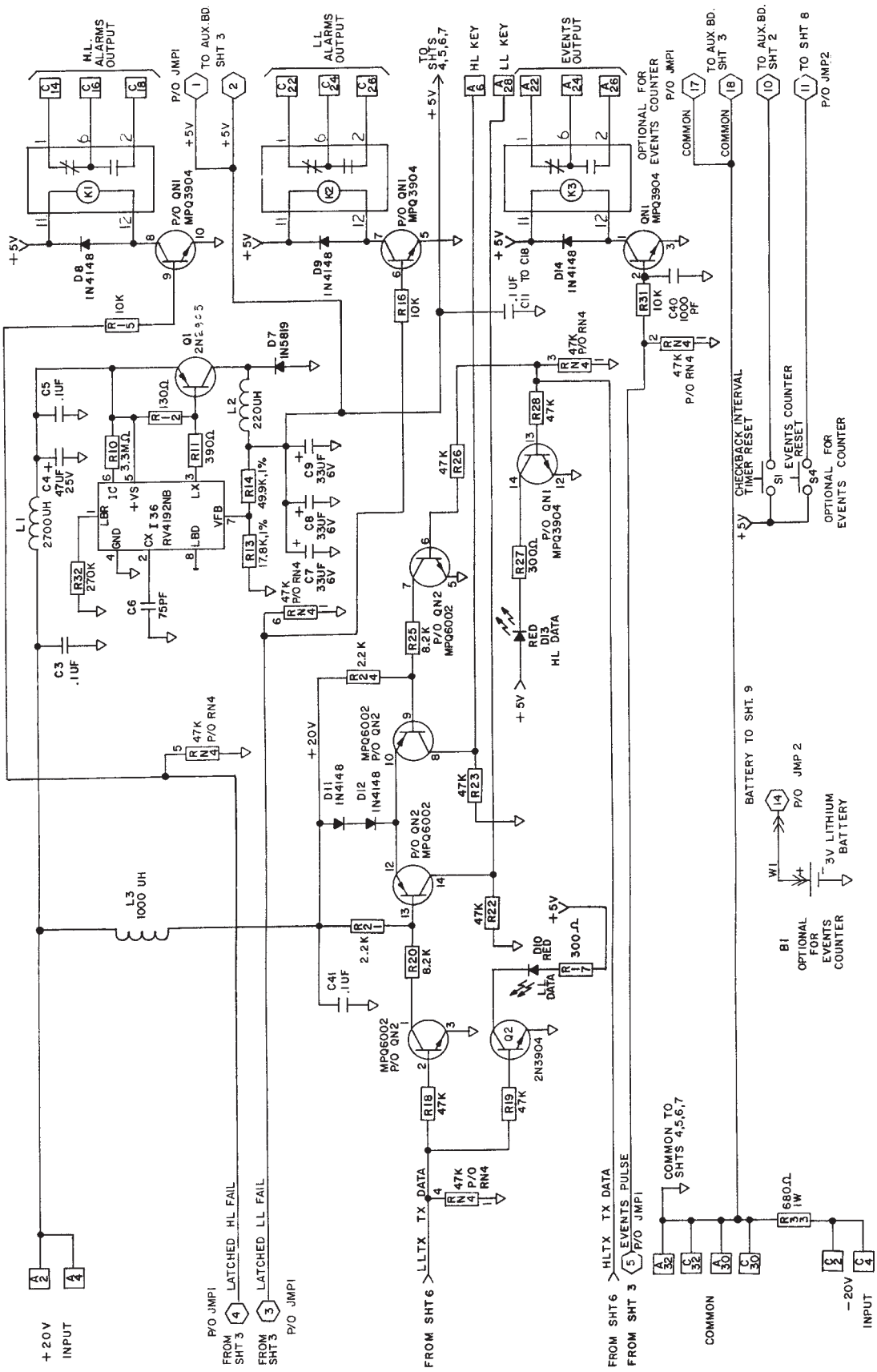


Figure 17–19. Master Checkback Schematic — Main Board. (1606C37, Sheet 5)

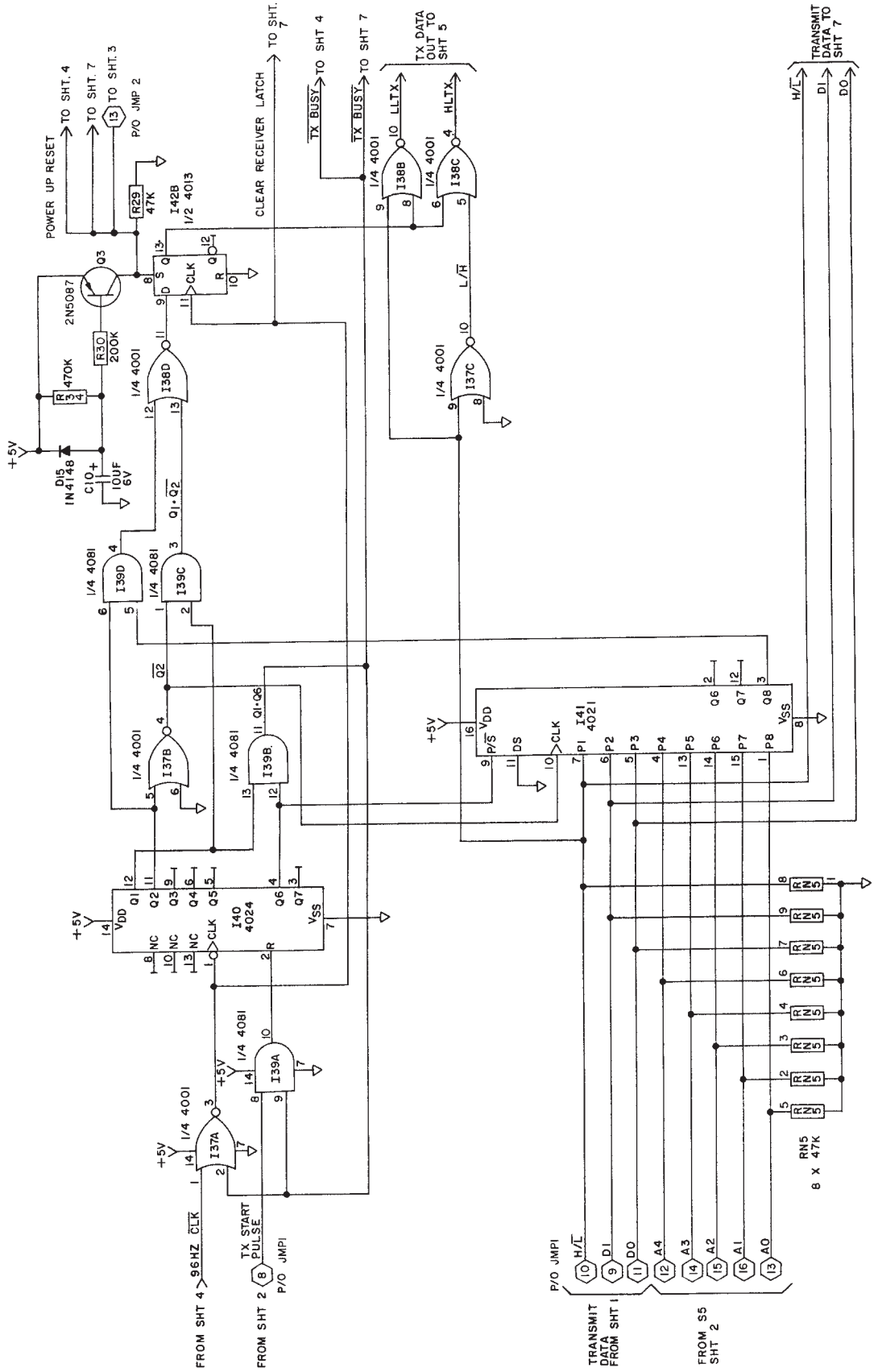


Figure 17–20. Master Checkback Schematic — Main Board. (1606C37, Sheet 6)

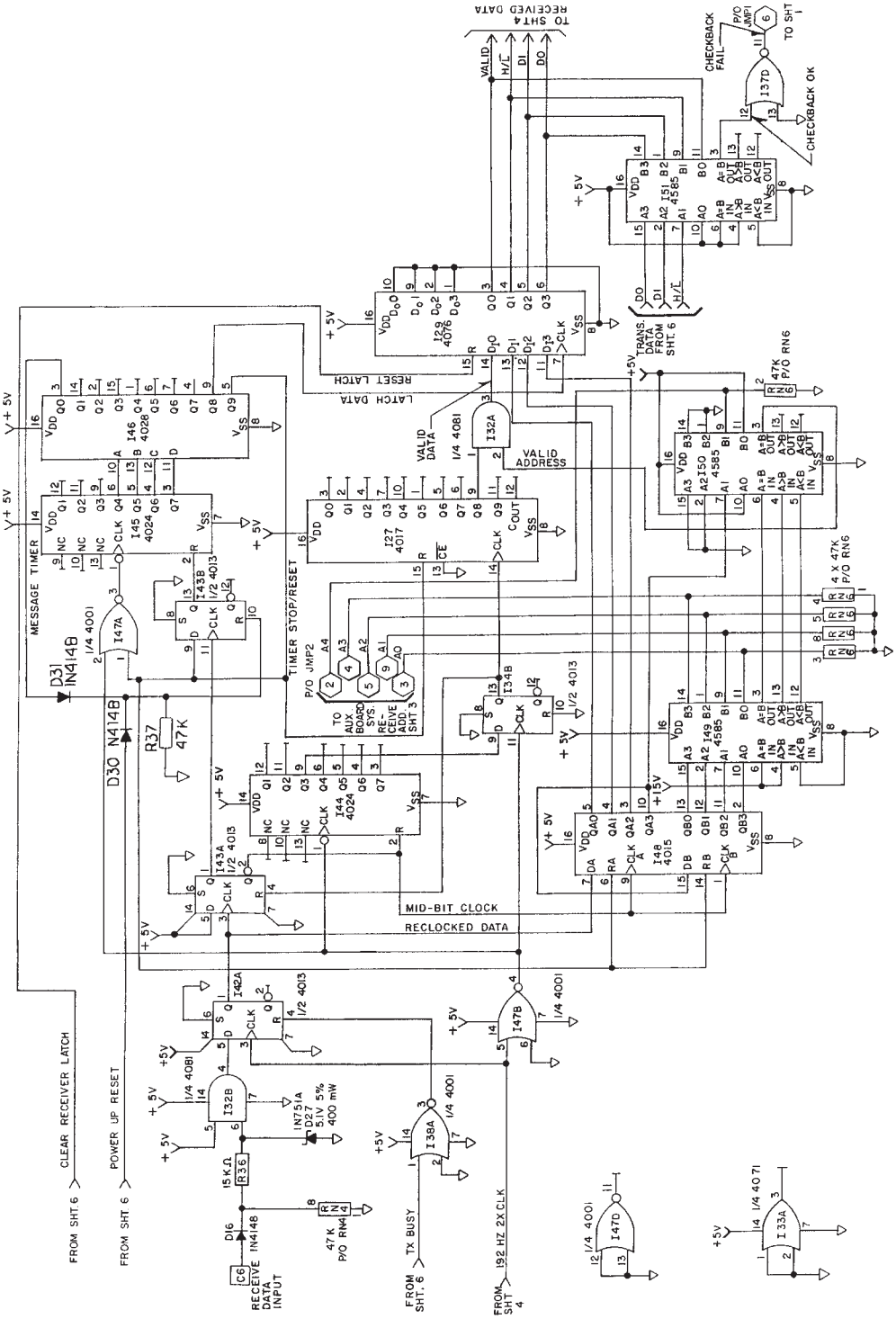


Figure 17–21. Master Checkback Schematic — Main Board. (1606C37, Sheet 7)

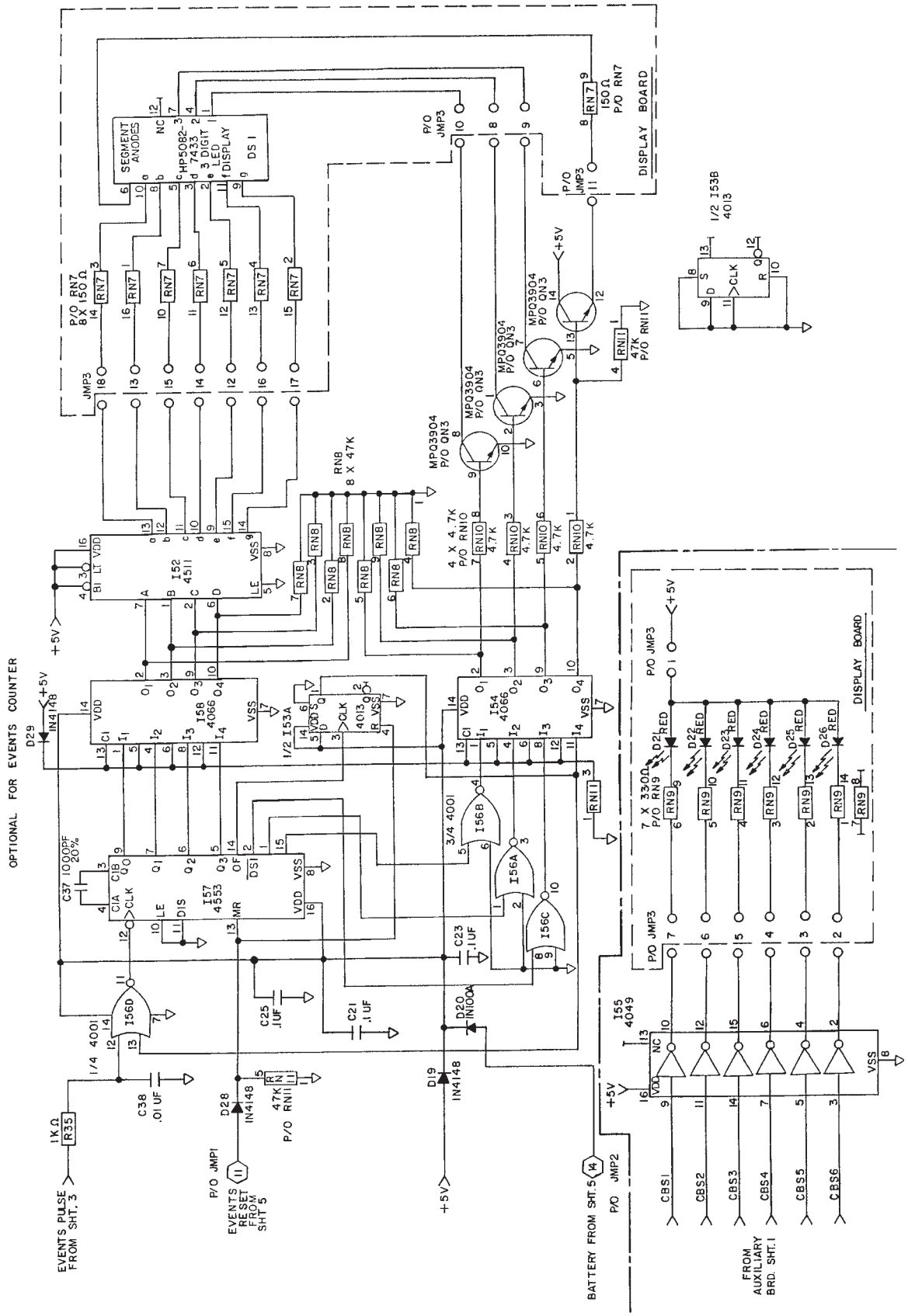


Figure 17–22. Master Checkback Schematic — Display Board. (1606C37, Sheet 8)

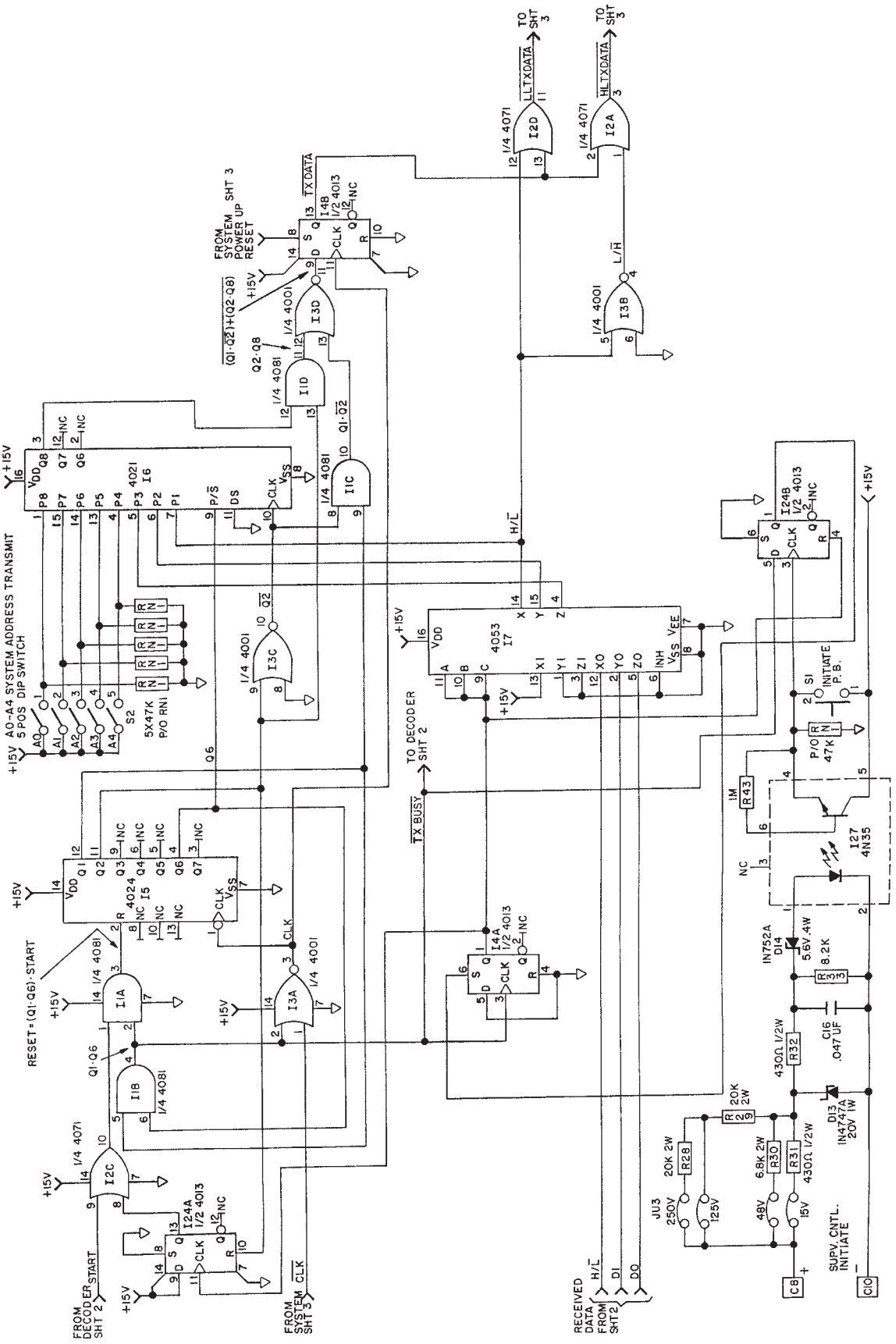


Figure 17–23. Remote Checkback Schematic — Encoder. (1606C38, Sheet 1)

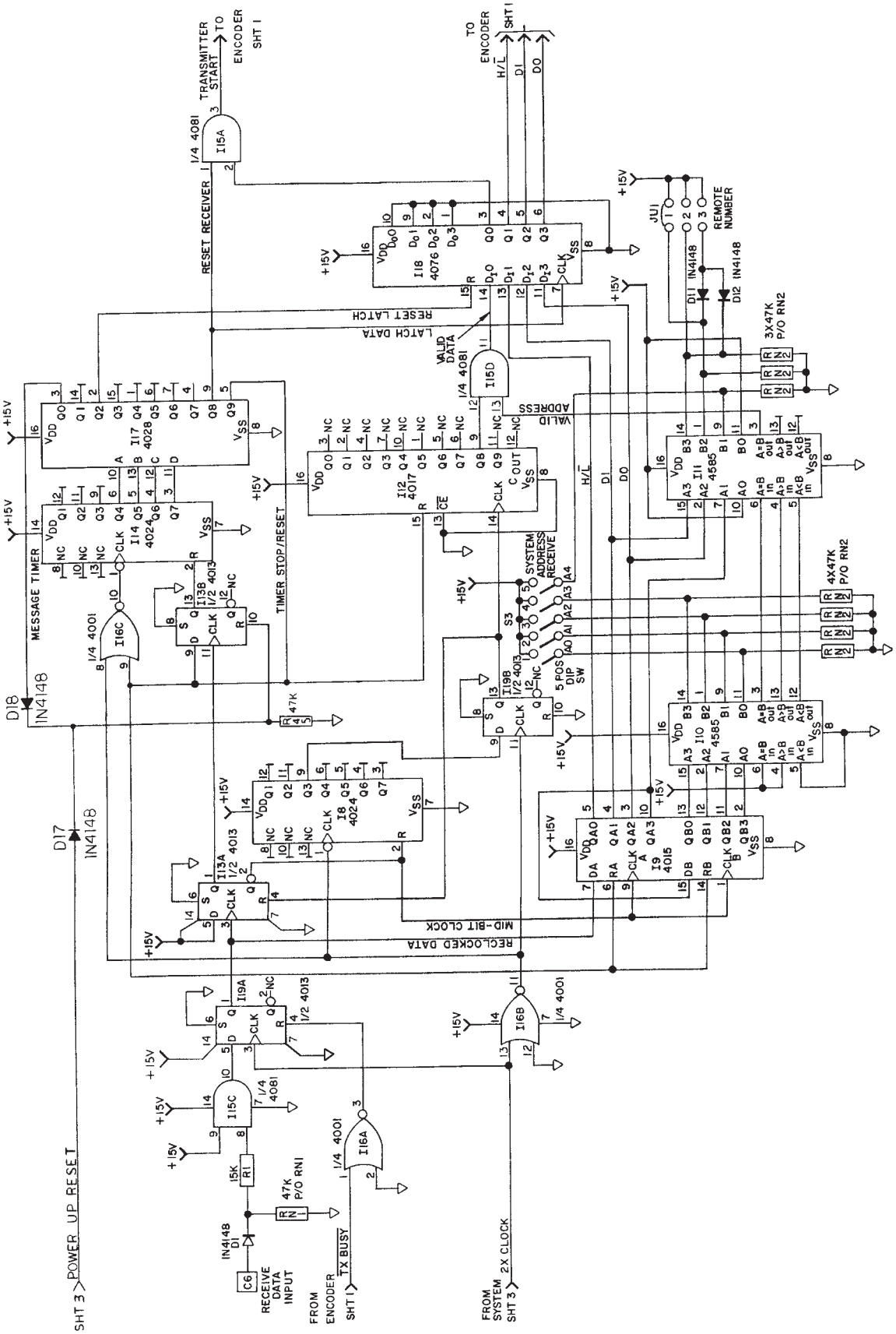


Figure 17–24. Remote Checkback Schematic — Decoder. (1606C38, Sheet 2)

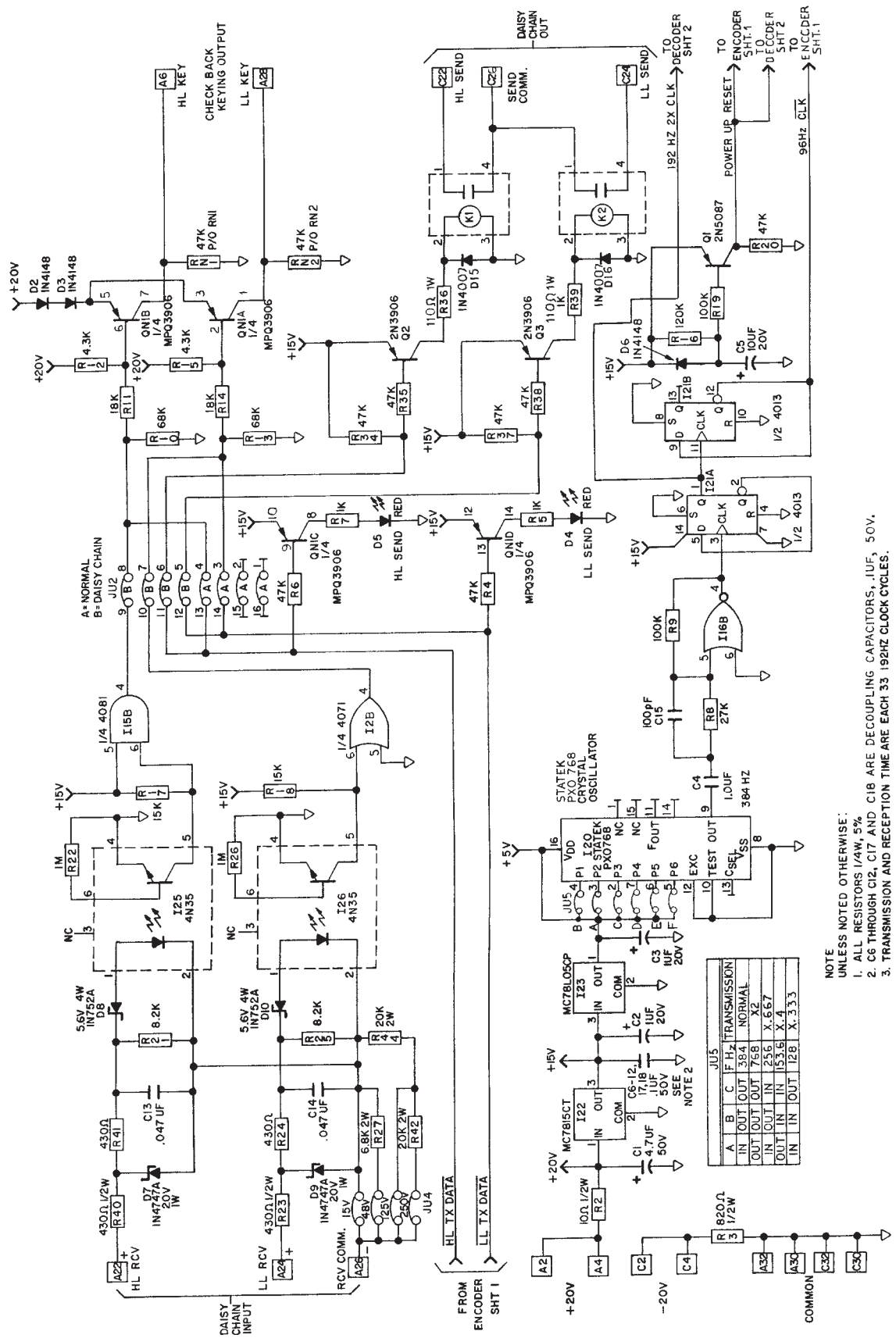


Figure 17–25. Remote Checkback Schematic — System. (1606C38, Sheet 3)

Table 17–4. Master Checkback Module Components. (1606C37)

Location	Style	Description	Group
BATTERIES			
B01	9648A03H01	3 V 75 MAH BR-2016	03
CAPACITORS			
C01	CF4702JL78	0.047 µF 5% 100 V MET POLYCARB	03,04
C02	CF4701GL70	4700 pF 2% 100 V MET POLYCARB	03,04
C03	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C04	CJ4705ME72	47 µF 20% 25 V MOLDED TANTALUM	03,04
C05	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C06	CR750AJV67	75 pF 5% 500 V DIPPED MICA	03,04
C07	CJ3305MA72	33 µF 20% 6 V MOLDED TANTALUM	03,04
C08	CJ3305MA72	33 µF 20% 6 V MOLDED TANTALUM	03,04
C09	CJ3305MA72	33 µF 20% 6 V MOLDED TANTALUM	03,04
C10	CJ1005MA72	10 µF 20% 6 V MOLDED TANTALUM	03,04
C11	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C12	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C13	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C14	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C15	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C16	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C17	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C18	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04
C19	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C20	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C21	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C22	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C23	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C24	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C25	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C26	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C27	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C28	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C29	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C30	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C31	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C32	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C33	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C34	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C35	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C36	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C37	CP1001ML65	1,000 pF 20% 100 V X7R MONO CERAMIC	05
C38	CP1002MH65	0.01 µF 20% 50 V X7R MONO CERAMIC	05
C39	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	05
C40	CP1001ML65	1,000 pF 20% 100 V X7R MONO CERAMIC	03,04
C41	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	03,04

Table 17–4. Master Checkback Module Components. (Cont'd)

Location	Style	Description	Group
CHOKES			
L01	3532A37H04	2,700 μH 10% 105 MA 32 OHMS	03,04
L02	3532A37H02	3443-56 220 μH .420 OHM 10%	03,04
L03	9646A07H49	1,000.0 μH 10%	03,04
CONNECTORS			
JMP1	3529A12H14	18 PIN SINGLE ROW HEADER	03,04
JMP1	3532A99H09	1000-218-2105 (18 POS)	05
JU1	3532A49H07	14 PIN	05
JMP2	3529A12H11	14 PIN SINGLE ROW HEADER	03,04
JMP2	3532A99H03	CONNECTOR 14 POS	05
JU2	3532A49H07	14 PIN	05
JMP3	3533A56H10	18 POSITIONS	05
JU3	3532A49H07	14 PIN	05
JU4	3532A49H07	14 PIN	05
JU5	3532A49H07	14 PIN	05
JU6	3532A49H07	14 PIN	05
JU8	3532A49H06	4 POSITION DOUBLE ROW	05
JU10	9640A47H01	3 POSITION	05,06
JU11	9640A47H01	3 POSITION	05,06
JU12	9640A47H01	3 POSITION	05,06
JU14	9640A47H01	3 POSITION	05,06
JU13	3532A49H08	18 PIN	05
JU15	3532A49H06	4 POSITION DOUBLE ROW	03,04
DIGITAL ICs			
I1	3527A09H10	MC14017BCP DECADE COUNTER	05
I2	3536A15H01	MC14071BCP QUAD 2-INPUT OR	05
I3	3536A15H01	MC14071BCP QUAD 2-INPUT OR	05
I4	9646A74H01	MC14075BCP TRIPLE 3-INPUT OR	05
I5	9646A74H01	MC14075BCP TRIPLE 3-INPUT OR	05
I6	3536A15H01	MC14071BCP QUAD 2-INPUT OR	05
I7	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	05
I8	9646A71H01	MC14099BCP 8-BIT ADDRESS LATCH	05
I9	3536A27H01	MC14569BCP DUAL PROG 4-BIT DWN-CTR	05
I10	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	05
I11	3536A17H01	MC14081BCP QUAD 2-INPUT AND	05
I12	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	05
I13	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	05
I14	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	05
I15	3536A27H01	MC14569BCP DUAL PROG 4-BIT DWN-CTR	05
I16	3535A14H01	MC14526BCP PROG 4-BIT BINARY DWN-CT	05

(Continued on next page.)

Table 17–4. Master Checkback Module Components. (Cont'd)

Location	Style	Description	Group
DIGITAL ICs (Cont'd)			
I17	3535A13H01	MC14040BCP 12-BIT BINARY COUNTER	05
I18	3535A14H01	MC14526BCP PROG 4-BIT BINARY DWN-CT	05
I19	3535A14H01	MC14526BCP PROG 4-BIT BINARY DWN-CT	05
I20	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	05
I21	3536A15H01	MC14071BCP QUAD 2-INPUT OR	05
I22	3536A17H01	MC14081BCP QUAD 2-INPUT AND	05
I23	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	05
I24	3536A15H01	MC14071BCP QUAD 2-INPUT OR	05
I25	3536A17H01	MC14081BCP QUAD 2-INPUT AND	05
I26	3535A13H01	MC14040BCP 12-BIT BINARY COUNTER	05
I27	3527A09H10	MC14017BCP DECADE COUNTER	03,04
I29	9646A72H01	MC14076BCP 4-BIT D-REGISTER	03,04
I30	9646A75H01	MC14585BCP 4-BIT MAG COMPARATOR.	03,04
I31	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	03,04
I32	3536A17H01	MC14081BCP QUAD 2-INPUT AND	03,04
I33	3536A15H01	MC14071BCP QUAD 2-INPUT OR	03,04
I34	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	03,04
I35	9642A78H02	PX0768 PROG. XTAL OSCILLATOR	03,04
I37	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	03,04
I38	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	03,04
I39	3536A17H01	MC14081BCP QUAD 2-INPUT AND	03,04
I40	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	03,04
I41	9646A70H01	MC14021BCP DUAL 4-BIT STATIC S R	03,04
I42	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	03,04
I43	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	03,04
I44	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	03,04
I45	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	03,04
I46	3533A85H01	MC14028BCP BCD-DECIMAL DECODER	03,04
I47	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	03,04
I48	9646A73H01	MC14015BCP DUAL 4-BIT STATIC S-R	03,04
I49	9646A75H01	MC14585BCP 4-BIT MAG COMPARATOR.	03,04
I50	9646A75H01	MC14585BCP 4-BIT MAG COMPARATOR.	03,04
I51	9646A75H01	MC14585BCP 4-BIT MAG COMPARATOR.	03,04
I52	9647A96H01	MC14511BCP BCD TO 7-SEG DECDR/DRVR	05
I53	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	05
I54	3534A28H01	MC14066BCP QUAD BILATERAL SWITCH	05
I55	3533A86H01	MC14049UBCP HEX INVERTER/BUFFER	05
I56	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	05
I57	9647A95H01	MC14553BCP 3-DIGIT BCD COUNTER	05
I58	3534A28H01	MC14066BCP QUAD BILATERAL SWITCH	05

Table 17–4. Master Checkback Module Components. (Cont'd)

Location	Style	Description	Group
DIODES			
D01	836A928H06	1N4148 75 V 0.01 A	05
D2	836A928H06	1N4148 75 V 0.01 A	05
D3	836A928H06	1N4148 75 V 0.01 A	05
D4	836A928H06	1N4148 75 V 0.01 A	05
D5	836A928H06	1N4148 75 V 0.01 A	05
D6	836A928H06	1N4148 75 V 0.01 A	05
D07	9648A05H02	1N5819 40 V 1 A SCHOTTKY	03,04
D8	836A928H06	1N4148 75 V 0.01 A	03,04
D9	836A928H06	1N4148 75 V 0.01 A	03,04
D11	836A928H06	1N4148 75 V 0.01 A	03,04
D12	836A928H06	1N4148 75 V 0.01 A	03,04
D14	836A928H06	1N4148 75 V 0.01 A	03,04
D15	836A928H06	1N4148 75 V 0.01 A	03,04
D16	836A928H06	1N4148 75 V 0.01 A	03,04
D19	836A928H06	1N4148 75 V 0.01 A	05
D20	182A881H07	1N100A 80 V 0.04 A GERMANIUM	05
D28	836A928H06	1N4148 75 V 0.01 A	05
D29	836A928H06	1N4148 75 V 0.01 A	05
D30	836A928H06	1N4148 75 V 0.01 A	03,04
D31	836A928H06	1N4148 75 V 0.01 A	03,04
JUMPERS			
JU1	3532A54H01	BLUE CLIP JUMPER	05
JU2	3532A54H01	BLUE CLIP JUMPER	05
JU3	3532A54H01	BLUE CLIP JUMPER	05
JU4	3532A54H01	BLUE CLIP JUMPER	05
JU5	3532A54H01	BLUE CLIP JUMPER	05
JU6	3532A54H01	BLUE CLIP JUMPER	05
JU07	3532A54H05	0.1 WIRE JUMPER	03,04
JU8	3532A54H01	BLUE CLIP JUMPER	05
JU9	3532A54H01	BLUE CLIP JUMPER	05
JU10	3532A54H01	BLUE CLIP JUMPER	05
JU11	3532A54H01	BLUE CLIP JUMPER	05
JU12	3532A54H01	BLUE CLIP JUMPER	05
JU13	3532A54H01	BLUE CLIP JUMPER	05
JU14	3532A54H01	BLUE CLIP JUMPER	05
LINEAR ICs			
I36	9648A15H01	RV4192NB POS ADJ VOLTREG 2-30 V 0.15	03,04
QN1	3533A64H01	MPQ3904 QUAD NPN ARRAY 40 V 0.2 A	03,04
QN2	3533A62H01	MPQ6002 QUAD PNP/NPN ARRAY 30 V 0.5 A	03,04
QN3	3533A64H01	MPQ3904 QUAD NPN ARRAY 40 V 0.2 A	05

(Continued on next page.)

Table 17–4. Master Checkback Module Components. (Cont'd)

Location	Style	Description	Group
OPTOELECTRONICS			
D10	3508A22H01	RED LED (EDGE MOUNT) 550-0406	03,04
D13	3508A22H01	RED LED (EDGE MOUNT) 550-0406	03,04
I28	774B936H01	4N35 OPTO-ISO.	03,04
RELAYS			
K01	3532A77H02	SPDT 5 V .5 A 310-OHM COIL PC MT	03,04
K02	3532A77H02	SPDT 5 V .5 A 310-OHM COIL PC MT	03,04
K03	3532A77H02	SPDT 5 V .5 A 310-OHM COIL PC MT	03
RESISTOR NETWORKS			
RN01	3533A81H14	7 COMM TERML 47 KILOHMS 2% SIP	05
RN02	3533A81H07	4 COMM TERML 47 KILOHMS 2% SIP	05
RN03	3533A81H02	8 COMM TERML 47 KILOHMS 2% SIP	05
RN04	3533A81H14	7 COMM TERML 47 KILOHMS 2% SIP	03,04
RN05	3533A81H02	8 COMM TERML 47 KILOHMS 2% SIP	03,04
RN06	3533A81H14	7 COMM TERML 47 KILOHMS 2% SIP	03,04
RN08	3533A81H02	8 COMM TERML 47 KILOHMS 2% SIP	05
RN10	3533A81H15	4 INDIVIDUAL 4.7 KILOHMS 2% SIP	05
RN11	3533A81H07	4 COMM TERML 47 KILOHMS 2% SIP	05
RN12	3533A81H07	4 COMM TERML 47 KILOHMS 2% SIP	05
RN13	3533A81H07	4 COMM TERML 47 KILOHMS 2% SIP	05
RESISTORS			
R01	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	03,04
R02	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	03,04
R03	RC6801J249	6.8 KILOHMS 5% 2 W CARBON COMP	03,04
R04	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	03,04
R05	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	03,04
R06	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	03,04
R07	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	03,04
R08	RB1004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	03,04
R09	RB2002JQB3	20 KILOHMS 5% 0.25 W CARBON FILM	03,04
R10	RB3304JQB3	3.3 MEGOHMS 5% 0.25 W CARBON FILM	03,04
R11	RB3900JQB2	390 OHMS 5% 0.25 W CARBON FILM	03,04
R12	RB1300JQB2	130 OHMS 5% 0.25 W CARBON FILM	03,04
R13	RM1782FQA9	17.8 KILOHMS 1% 0.25 W METAL FILM	03,04
R14	RM4992FQA9	49.9 KILOHMS 1% 0.25 W METAL FILM	03,04
R15	RB1002JQB3	10 KILOHMS 5% 0.25 W CARBON FILM	03,04
R16	RB1002JQB3	10 KILOHMS 5% 0.25 W CARBON FILM	03,04
R17	RB3000JQB2	300 OHMS 5% 0.25 W CARBON FILM	03,04
R18	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R19	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R20	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	03,04
R21	RB2201JQB2	2.2 KILOHMS 5% 0.25 W CARBON FILM	03,04
R22	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R23	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R24	RB2201JQB2	2.2 KILOHMS 5% 0.25 W CARBON FILM	03,04

Table 17–4. Master Checkback Module Components. (Cont'd)

Location	Style	Description	Group
RESISTORS (Cont'd)			
R25	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	03,04
R26	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R27	RB3000JQB2	300 OHMS 5% 0.25 W CARBON FILM	03,04
R28	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R29	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R30	RB2003JQB3	200 KILOHMS 5% 0.25 W CARBON FILM	03,04
R31	RB1002JQB3	10 KILOHMS 5% 0.25 W CARBON FILM	03,04
R32	RB2703JQB3	270 KILOHMS 5% 0.25 W CARBON FILM	03,04
R33	RC6800J167	680 OHMS 5% 1 W CARBON COMP	03,04
R34	RB4703JQB3	470 KILOHMS 5% 0.25 W CARBON FILM	03,04
R35	RB1001JQB2	1.0 KILOHMS 5% 0.25 W CARBON FILM	05
R36	RB1502JQB3	15 KILOHMS 5% 0.25 W CARBON FILM	03,04
R37	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	03,04
R38	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	05
SWITCHES			
SW01	9646A57H01	SPST PUSH BUTTON	03,04
SW02	775B517H02	8 POSITION DIP	05
SW03	9646A57H01	SPST PUSH BUTTON	03,04
SW04	9646A57H01	SPST PUSH BUTTON	03
SW05	775B517H03	5 POSITION DIP	05
SW06	775B517H03	5 POSITION DIP	05
SW07	775B77H02	8 POSITION DIP	05
SW08	775B517H03	5 POSITION DIP	05
TRANSISTORS			
Q01	762A672H10	2N2905A 60 V 0.6 A 0.6 W PNP	03,04
Q02	3509A35H05	2N3904 40 V 0.2 A 0.625 W NPN	03,04
Q03	3509A35H11	2N5087 50 V 0.05 A 0.35 W PNP	03,04
ZENERS			
D17	849A487H01	1N4747A 20 V 5% 1 W	03,04
D18	186A797H12	1N752A 5.6 V 5% 0.4 W	03,04
D27	862A606H06	1N751A 5.1 V 5% 0.4 W	03,04

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Table 17–5. Remote Checkback Module Components. (1606C38)

Location	Style	Description	Group
CAPACITORS			
C01	CJ4704MH72	4.7 µF 20% 50 V MOLDED TANTALUM	01
C02	CJ1004MD72	1.0 µF 20% 20 V MOLDED TANTALUM	01
C03	CJ1004MD72	1.0 µF 20% 20 V MOLDED TANTALUM	01
C04	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C05	CJ1005MD72	10 µF 20% 20 V MOLDED TANTALUM	01
C06	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C07	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C08	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C09	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C10	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C11	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C12	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C13	CF4702JL78	0.047 µF 5% 100 V MET POLYCARB	01
C14	CF4702JL78	0.047 µF 5% 100 V MET POLYCARB	01
C15	CP1000KHZZ	100 pF 10% 50 V X7R MONO CERAMIC	01
C16	CF4702JL78	0.047 µF 5% 100 V MET POLYCARB	01
C17	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
C18	CP1003MH65	0.1 µF 20% 50 V X7R MONO CERAMIC	01
DIGITAL ICs			
I01	3536A17H01	MC14081BCP QUAD 2-INPUT AND	01
I02	3536A15H01	MC14071BCP QUAD 2-INPUT OR	01
I03	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	01
I04	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	01
I05	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	01
I06	9646A70H01	MC14021BCP DUAL 4-BIT STATIC S R	01
I07	3533A70H01	MC14053BCP TRIPLE 2-CH ANALOG MUX	01
I08	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	01
I09	9646A73H01	MC14015BCP DUAL 4-BIT STATIC S-R	01
I10	9646A75H01	MC14585BCP 4-BIT MAG COMPARATOR.	01
I11	9646A75H01	MC14585BCP 4-BIT MAG COMPARATOR.	01
I12	3527A09H10	MC14017BCP DECADE COUNTER	01
I13	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	01
I14	9647A46H01	MC14024BCP 7-STAGE RIPPLE CNTR	01
I15	3536A17H01	MC14081BCP QUAD 2-INPUT AND	01
I16	3536A51H01	MC14001BCP QUAD 2-INPUT NOR	01
I17	3533A85H01	MC14028BCP BCD-DECIMAL DECODER	01
I18	9646A72H01	MC14076BCP 4-BIT D-REGISTER	01
I19	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	01
I20	9642A78H02	PX0768 PROGRAMMABLE XTAL OSC.	01
I21	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	01
I24	3535A12H01	MC14013BCP DUAL D FLIP-FLOP	01

Table 17–5. Remote Checkback Module Components. (Cont'd)

Location	Style	Description	Group
DIODES			
D01	836A928H06	1N4148 75 V 0.01 A	01
D02	836A928H06	1N4148 75 V 0.01 A	01
D03	836A928H06	1N4148 75 V 0.01 A	01
D06	836A928H06	1N4148 75 V 0.01 A	01
D11	836A928H06	1N4148 75 V 0.01 A	01
D12	836A928H06	1N4148 75 V 0.01 A	01
D15	836A928H06	1N4007 1,000 V 1 A	01
D16	836A928H06	1N4007 1,000 V 1 A	01
D17	836A928H06	1N4148 75 V 0.01 A	01
D18	836A928H06	1N4148 75 V 0.01 A	01
JUMPERS			
JU05	862A478H01	ZERO OHM RESISTOR	01
LINEAR ICs			
I22	3535A22H01	MC7815CT POS VOLTREG 15 V 4% 1 A	01
I23	3534A39H02	MC78L05CP POS VOLTREG 5 V 5% 0.1 A	01
QN01	3533A63H01	MPQ3906 QUAD PNP ARRAY 40 V 0.2 A	01
OPTOELECTRONICS			
D04	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01
D05	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01
I25	774B936H01	4N35 OPTO-ISO.	01
I26	774B936H01	4N35 OPTO-ISO.	01
I27	774B936H01	4N35 OPTO-ISO.	01
RELAYS			
K01	9647A91H01	HE3351A0500 REED HV 1 A N.O.	01
K02	9647A91H01	HE3351A0500 REED HV 1 A N.O.	01
RESISTOR NETWORKS			
RN01	3533A81H02	8 COMM TERML 47 KILOHMS 2% SIP	01
RN02	3533A81H02	8 COMM TERML 47 KILOHMS 2% SIP	01

(Continued on next page.)

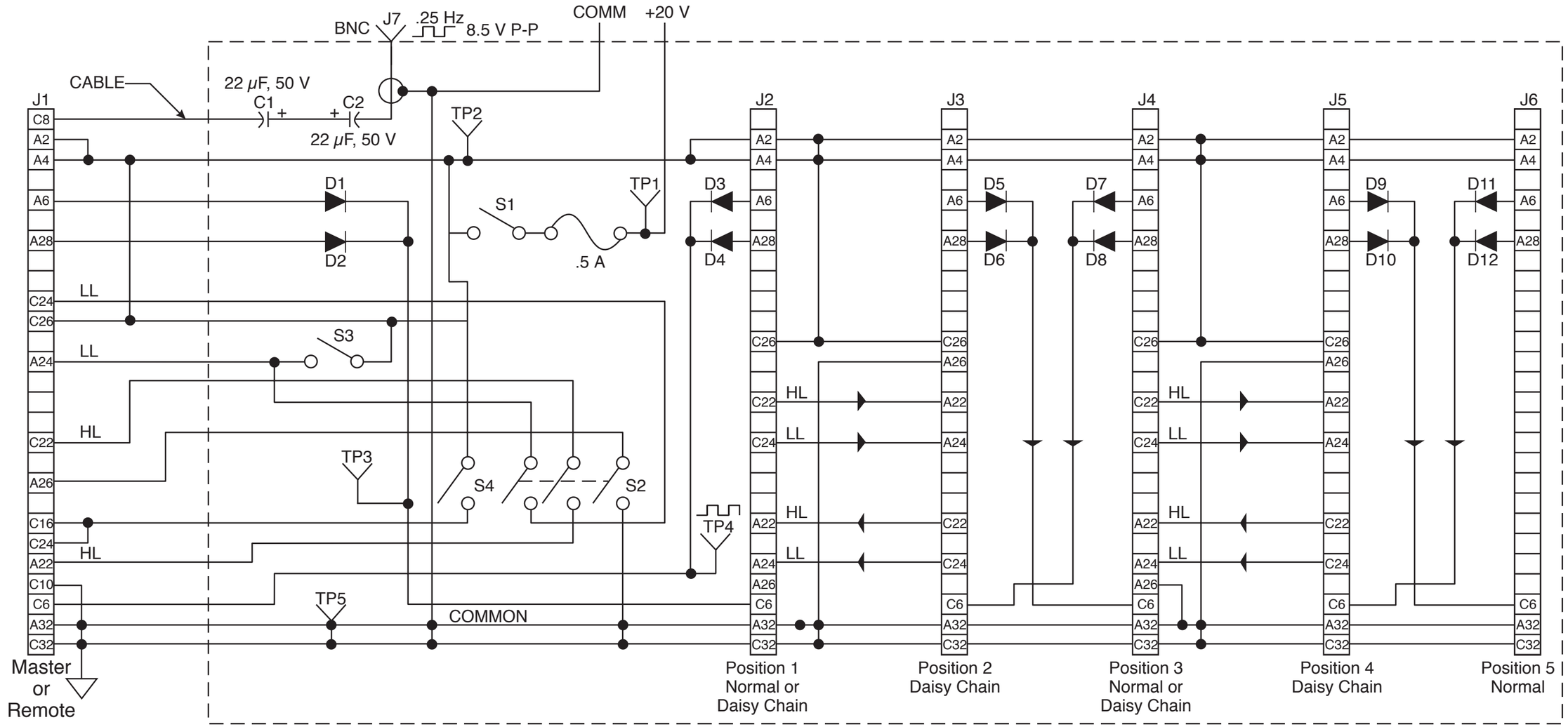
Table 17–5. Remote Checkback Module Components. (Cont'd)

Location	Style	Description	Group
RESISTORS			
R01	RB1502JQB3	15 KILOHMS 5% 0.25 W CARBON FILM	01
R02	RB100AJHL8	10 OHMS 5% 0.5 W CARBON FILM	01
R03	RB8200JHL7	820 OHM .50 W 5% CARBON FILM	01
R04	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R05	RB1001JQB	1.0 KILOHMS 5% 0.25 W CARBON FILM	01
R06	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R07	RB1001JQB2	1.0 KILOHMS 5% 0.25 W CARBON FILM	01
R08	RB2702JQB3	27 KILOHMS 5% 0.25 W CARBON FILM	01
R09	RB1003JQB3	100 KILOHMS 5% 0.25 W CARBON FILM	01
R10	RB6802JQB3	68 KILOHMS 5% 0.25 W CARBON FILM	01
R11	RB1802JQB3	18 KILOHMS 5% 0.25 W CARBON FILM	01
R12	RB4301JQB2	4.3 KILOHMS 5% 0.25 W CARBON FILM	01
R13	RB6802JQB3	68 KILOHMS 5% 0.25 W CARBON FILM	01
R14	RB1802JQB	18 KILOHMS 5% 0.25 W CARBON FILM	01
R15	RB4301JQB2	4.3 KILOHMS 5% 0.25 W CARBON FILM	01
R16	RB1203JQB3	120 KILOHMS 5% 0.25 W CARBON FILM	01
R17	RB1502JQB3	15 KILOHMS 5% 0.25 W CARBON FILM	01
R18	RB1502JQB	15 KILOHMS 5% 0.25 W CARBON FILM	01
R19	RB1003JQB3	100 KILOHMS 5% 0.25 W CARBON FILM	01
R20	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R21	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	01
R22	RB1004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	01
R23	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R24	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R25	RB8201JQB	8.2 KILOHMS 5% 0.25 W CARBON FILM	01
R26	RB1004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	01
R27	RC6801J249	6.8 KILOHMS 5% 2 W CARBON COMP	01
R28	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R29	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R30	RC6801J249	6.8 KILOHMS 5% 2 W CARBON COMP	01
R31	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R32	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R33	RB8201JQB2	8.2 KILOHMS 5% 0.25 W CARBON FILM	01
R34	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R35	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R36	RC1100J167	110 OHMS 5% 1 W CARBON COMP	01
R37	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R38	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01
R39	RC1100J167	110 OHMS 5% 1 W CARBON COMP	01
R40	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R41	RB4300JHL8	430 OHMS 5% 0.5 W CARBON FILM	01
R42	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R43	RB1004JQB3	1.0 MEGOHMS 5% 0.25 W CARBON FILM	01
R44	RC2002J249	20 KILOHMS 5% 2 W CARBON COMP	01
R45	RB4702JQB3	47 KILOHMS 5% 0.25 W CARBON FILM	01

Table 17–5. Remote Checkback Module Components. (Cont'd)

Location	Style	Description	Group
SWITCHES			
SW01	9646A57H01	SPST PUSH BUTTON	01
SW02	775B517H03	5 POSITION DIP	01
SW03	775B517H03	5 POSITION DIP	01
TRANSISTORS			
Q01	3509A35H11	2N5087 50 V 0.05 A 0.35 W PNP	01
Q02	3509A35H0	2N3906 40 V 0.2 A 0.625 W PNP	01
Q03	3509A35H06	2N3906 40 V 0.2 A 0.625 W PNP	01
ZENERS			
D07	849A487H01	1N4747A 20 V 5% 1 W	01
D08	186A797H12	1N752A 5.6 V 5% 0.4 W	01
D09	849A487H01	1N4747A 20 V 5% 1 W	01
D10	186A797H12	1N752A 5.6 V 5% 0.4 W	01
D13	849A487H01	1N4747A 20 V 5% 1 W	01
D14	186A797H12	1N752A 5.6 V 5% 0.4 W	01

USER NOTES



Note: All diodes are 1N4003 unless otherwise specified.

Figure 17–26. TC–10B Checkback Test Fixture Schematic (1498B95)

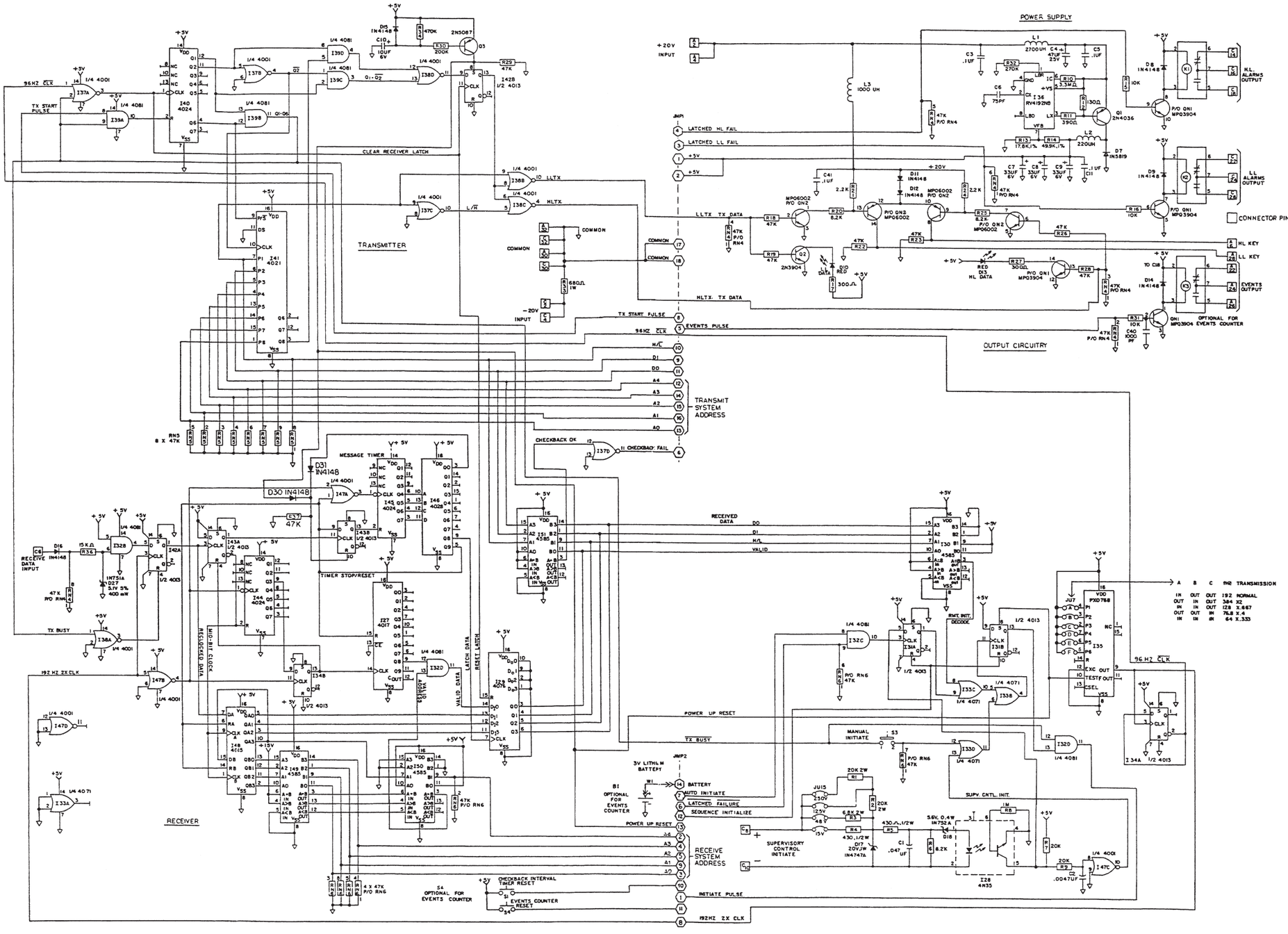


Figure 17–27. TC–10B Master Checkback Main Board (2404F92)

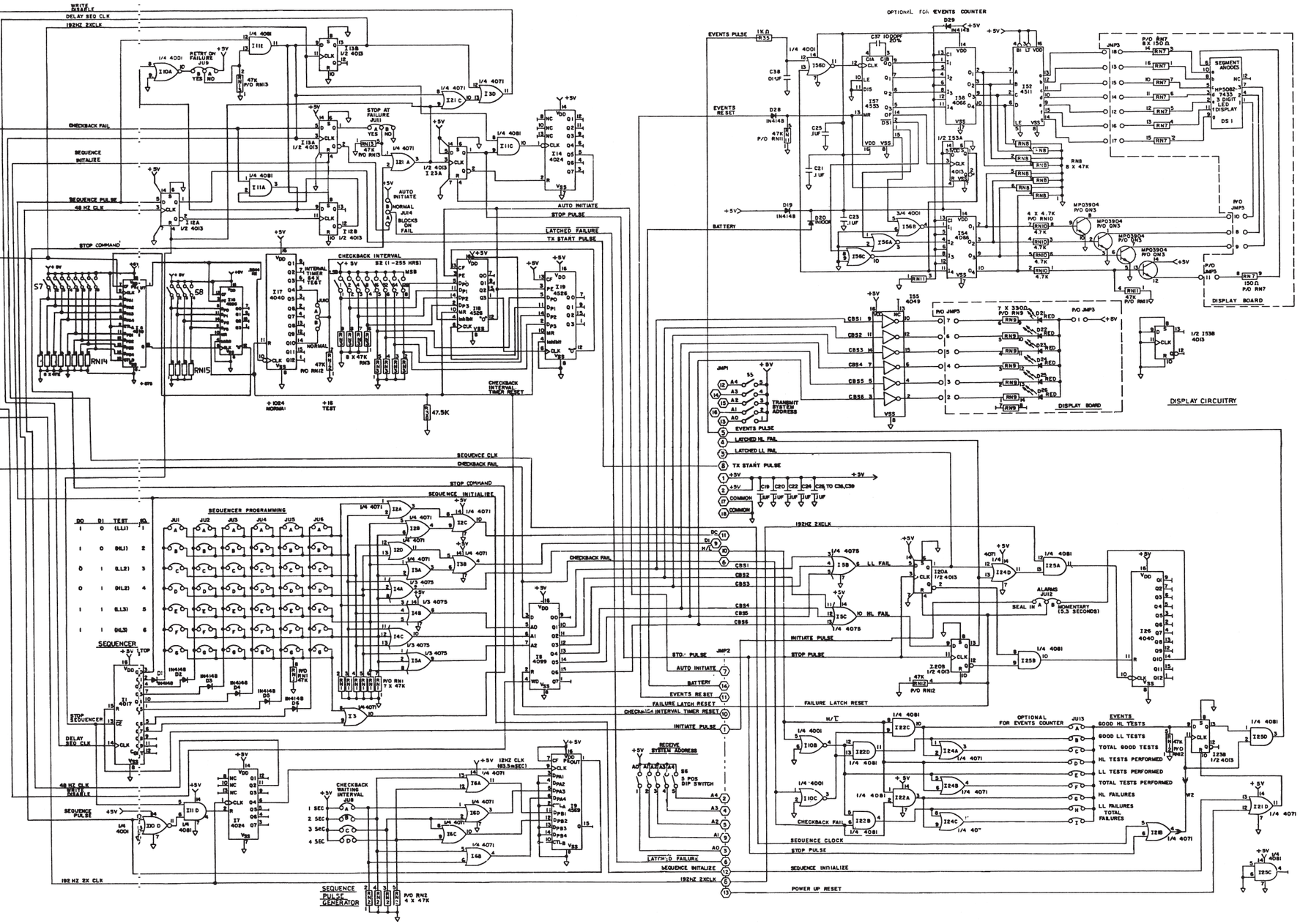


Figure 17–28. TC–10B Master Checkback Auxiliary Board. (2404F58)

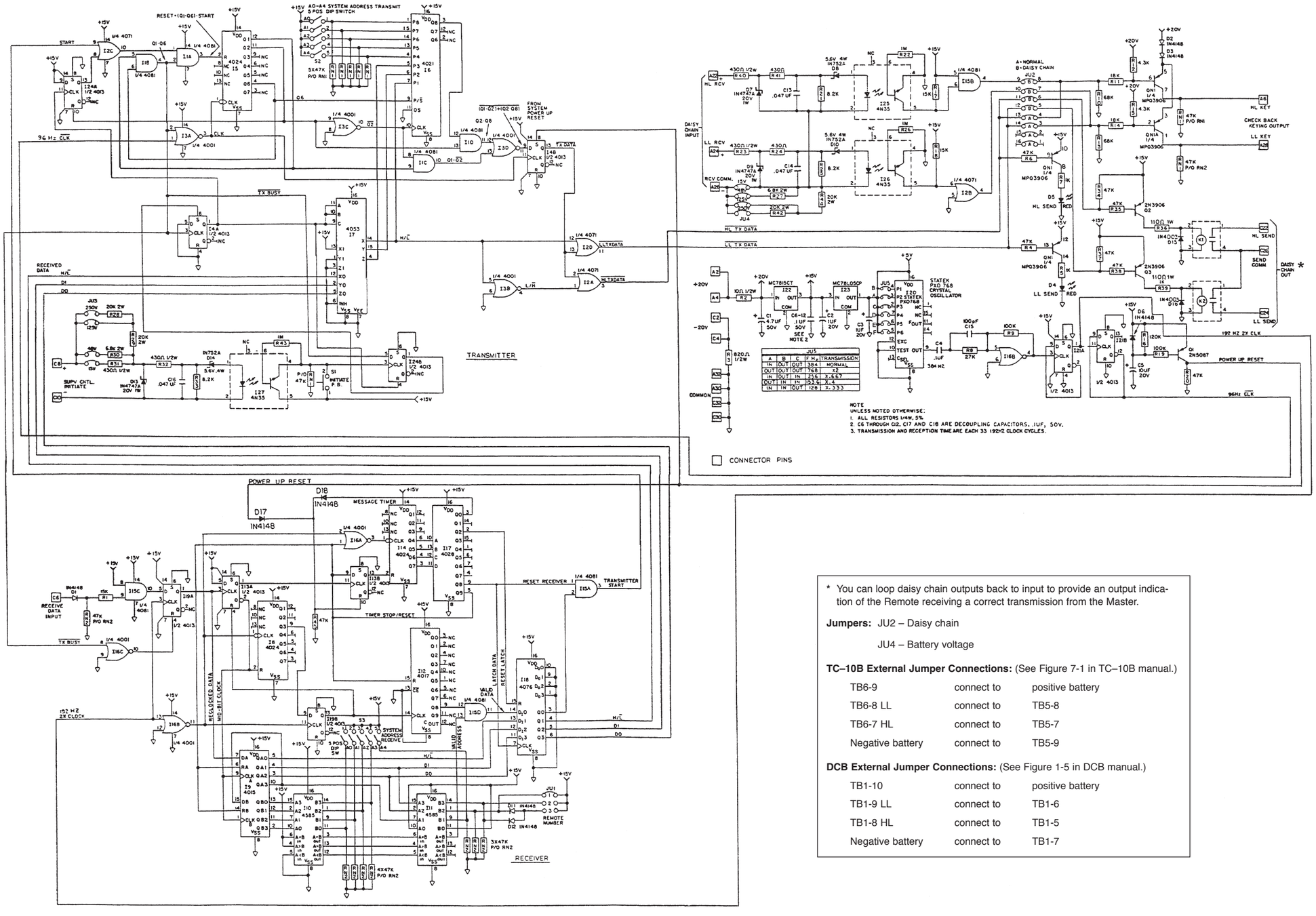


Figure 17–29. TC–10B Remote Checkback Board. (2404F93)

Chapter 18. Optional Voice Adapter Module

Schematic	1606C39-16
Parts List	1606C39-16

18.1 Voice Adapter Module Description

The Voice Adapter Module is designed to provide voice communications between terminals of the TC–10B/TCF–10B carrier systems. This module also provides signaling. Voice communication is provided on a half-duplex basis for the TC–10B, and a full-duplex basis for the TCF–10B.

18.1.1 TC–10B Operation

The Receiver in the TC–10B system outputs 5.02 MHz IF to the Voice Adapter, which is then filtered, AGC amplified, and detected. The detected audio is then amplified and received at the handset. You can connect the handset (with a "push-to-talk" switch) to the TC–10B in three different ways:

1. Plug the handset into the TC–10B Voice Adapter Module at the front panel "HANDSET" jack.
2. Connect the handset remotely, through a jack, to the TC–10B rear panel (terminal TB5).
3. Connect the hookswitch assembly (which supports a handset) remotely to the TC–10B rear panel (terminal TB5).

You initiate signaling by pressing the push-to-talk switch on the handset. You may terminate ringing, at the other end of the system, in four different ways (depending on the configuration you are using):

1. When a handset is plugged into the TC–10B Voice Adapter Module front panel "HANDSET" jack, it activates the alarm cutoff relay.
2. When a handset is connected, remotely, through a jack to the TC–10B rear panel (see Figure 18-4), the remote jack interrupts the alarm circuit.
3. When a handset is removed from its hook-switch; the hookswitch assembly being connected remotely to the TC–10B rear panel (see Figure 18-4), the hookswitch contacts interrupt the alarm circuit.
4. When a handset is used in combination with a hookswitch, lifting the handset and plugging in the handset interrupts the alarm circuit (see Figure 18-4).

When using the TC–10B with voice, refer to Figure 18-5 for the alarm cutoff circuit.

18.1.2 TCF–10B Operation

In the TCF–10B system, the receiver outputs 5.02 MHz IF to the Voice Adapter, which is then filtered, AGC amplified, and detected. The detected audio is then amplified and received at the handset. You can connect the handset to the TCF–10B in the following ways (a hookswitch assembly is required for remote TCF–10B operation):

1. Remote Handset Configuration

   Cradle a handset without a push-to-talk switch on a hookswitch assembly in a location remote from the TCF–10B Voice Adapter Module. Connect the hookswitch assembly in series with the alarm circuit, as well as to the TCF–10B rear panel terminal block TB5 (see Figure 18-4 and Figure 18-5).

   Install a separate calling pushbutton in the remote location, near the handset.

   Initiate signaling at the remote location by lifting the handset from the hookswitch assembly and pressing the calling pushbutton.

2. Local Handset Configuration

   Plug a handset without a push-to-talk switch into the front panel "HANDSET" jack of the Voice Adapter Module.

   Connect the alarm circuit per Figure 18-4 and Figure 18-5.

Initiate signaling by plugging the handset into the module assembly and pressing the calling push-button on the Voice Adapter (see Figure 1-1, "Calling PB").

If a handset with a Push-to-Talk switch is used in either configuration (above), you initiate signalling by lifting the handset from the hook-switch assembly and pressing the Push-to-Talk switch and the Calling pushbutton simultaneously.

18.1.3 Electrical Characteristics

The Voice Adapter Module's electrical characteristics are shown in Table 18-1.

Table 18–1. Voice Adapter Module Electrical Characteristics.

Operating Temp Range	-20° to +60° C (Ambient)
Audio Frequency Response	300 to 2,000 Hz (-3 dB)
Receiver Sensitivity	-74 dBm (50 ohm)
AGC Dynamic Range	40 dB min Audio output ± 0.5. DB for R.F. level change -74 dBm to -34 dBm
Compandor	Jumper selectable (IN/OUT)
TCF Signaling Tone	370 Hz ±50 Hz
TCF Signaling Tone Detector	370 Hz ± 50 Hz
Transmit Audio	3.2 Vp-p (in limit) into 600 ohm
Receive Audio Squelch	When RF input is below -80 dBm (Also jumper selectable to squelch with "push-to-talk" switch)
Powering	Module powered from +20 V, common, and -20 V power supply. Supply current is approximately 50 mA from each supply.
External Handset & Signaling Inputs	Must meet IEEE impulse and IEEE SWC tests (ANSI C37.90.1).
Alarm Terminals	Must pass 2,500 Vdc hi-pot for one minute (normal open/normal closed, jumper selectable).

18.2 Voice Adapter Panel Controls

18.2.1 Voice Adapter Control Panel

(This panel is shown in Figure 1-1.)

Operator controls are provided as follows:

Calling Pushbutton ("Calling PB")

Used with TCF–10B only to activate signaling oscillator.

Alarm/Alarm-Cutoff LED ("Alarm/Alarm Cutoff")

Indicates when Alarm/Alarm Cutoff relay is activated.

Receive Audio Level Adjustment ("Receive Audio", R24)

Adjusts the receive audio level.

Microphone Sensitivity Adjustment ("Mic. Sens", R63)

Sets the audio level output to the modulator.

Handset Jack ("Handset", TJ1)

(The handset schematic is shown in Figure 18-8.)

18.2.2 Voice Terminal Block on Rear Panel

(This panel is shown in Figure 3-1.)

Connections are as follows:

- Common
- Signaling input (external calling switch, to be returned to common when signaling).
- Alarm Cutoff signal (2 contacts: NO or NC).
- External receiver output.
- External microphone input.

18.3 Voice Adapter PC Board

(This board is shown in Figure 18-1.)

Operator controls are provided, as follows:

JU1 Receiver Squelch (IN/OUT). When the jumper is "IN", voice keying squelches the receive audio signal.

JU2/
JU3 Compandor (IN/OUT) When the jumper is "IN", the audio is compandored; when the jumper is "OUT", the audio is not compandored. We generally recommend that you use companding, as it improves the signal-to-noise performance.

JU4 Signaling (TC/TCF) When jumper is set for "TC", and handset is plugged into handset jack, the alarm cutoff from the handset jack will cause the relay to operate. When jumper is set for "TCF", the presence of a signaling tone will operate the relay.

JU5 Alarm Contacts (NO/NC) When jumper is set in "NO" position, and relay is de-energized, the alarm contacts will be "OPEN". When jumper is in "NC" position, and relay is de-energized, the alarm contacts will be "CLOSED".

18.4 Voice Adapter Circuit Description

18.4.1 Receiver

The RF input to the Voice Adapter is a 5.02-MHz IF signal from the Receiver Module, which is filtered by FL1, amplified by Q1, and input to I1 (an AGC amplifier). The I1 output is filtered by FL2, with Q2 operating as a buffer to drive the AM Detector (I2), which provides a demodulated audio output, plus a dc signal as input to the comparator (I3/1,2,3). Potentiometer R41 provides an adjustable reference and is factory set. The output of I3 controls the gain of the AGC amplifier (I1).

The audio output (from I2) will be squelched by the Audio Squelch circuit (I6) if the RF input (5.02 MHz) is below -85 dBm. This is accomplished by comparator (I3/5,6,7) which monitors the AGC central voltage (see Figure 18-3).

The audio output will also be squelched, with jumper JU1 "IN", when the transmitter is keyed. The front panel potentiometer RECEIVER AUDIO (R24) provides for field adjustment of the Receive Audio level when you adjust the input level to Audio Output Amplifier (I3/8,9,10). This amplified output is passed through an output protection circuit (R34, Z1) to the HANDSET jack (TJ1), or to a remote handset connected to terminal block (TB5) on the rear panel.

18.4.2 Audio Transmit

The Current Limiter, comprising Q4, Q5, and R72 (see Figure 18-3) provides approximately 22 mA to the handset microphone, when the push-to-talk switch in the handset is pushed. Front panel potentiometer MIC. SENS (R63) provides for adjustment of the level of audio voice signals from the microphone. These signals are input to the 2.2 kHz lowpass filter (I4/1,2,3), which attenuates frequencies above 2200 Hz. The output of I4 is input to the Output Limiter (I4/12,13,14), according to the following conditions:

- If JU2 is "OUT", input to I4(13) is direct
- If JU2 is "IN", input to I4(13) is through compressor (I5)

I4 outputs (through pin A-28) provide a maximum signal of 3.2 Vp-p into the 600 ohm input impedance of the Transmitter Module.

18.4.3 TC–10B/TCF–10B Signaling

Jumper JU4 selects either the TC–10B or the TCF–10B signaling operation.

TC–10B Signaling

Set jumper JU4 to the "TC" position. Also set jumper JU5 to "NC".

Initiate signaling by pressing the push-to-talk switch on the handset. Signals are detected by I7 and Q6, which signal a Voice-Key level to the Keying Module.

You may terminate ringing in two different ways (depending on the configuration used at the other end of the system):

1. By plugging the handset into the front panel "HANDSET" jack of the Voice Adapter Module, Relay K-1 is energized, illuminating the front control panel LED "Alarm/Alarm Cutoff"; the normally-closed contacts are opened and the alarm is interrupted.
2. When using a remotely-connected handset. The alarm contacts from the Voice Adapter (TB5) are wired in series with the Level Detector (TB2) contacts. When a carrier signal is received from a remote system, Level Detector (TB2) contacts close, providing an alarm signal. You can interrupt the alarm in the following ways:
   - By plugging the handset into a jack, which is connected remotely to the TC–10B rear panel (TB5); the jack contacts interrupt the alarm (see Figure 18-4, top scheme)
   - By lifting the handset from the hookswitch assembly, which is connected remotely to TB5; the hookswitch contacts interrupt the alarm (see Figure 18-4, bottom scheme)

TCF–10B Signaling

Set jumper JU4 to the "TCF" position. Also, set jumper JU5 to the "NO" position.

You initiate signaling by pressing the calling pushbutton (see section 18.1.2 TCF–10B Operation for the procedure). The signaling tone oscillator will operate and send a 370 Hz signaling tone to the Transmitter (at the originating end).

At the terminating end of the system, the receiver sends the signaling tone to the Signaling Tone Detector (filtered by I4,8,9,10 and detected by I4/5,6,7), causing relay K1 to operate, closing the alarm contacts.

The normally-open (N.O.) alarm relay contacts are wired in series with the external normally-closed hookswitch contacts (see Figure 18-6). The normally-closed contacts allow alarm signaling to be interrupted when the handset (at the terminating end) is removed from its hookswitch assembly.

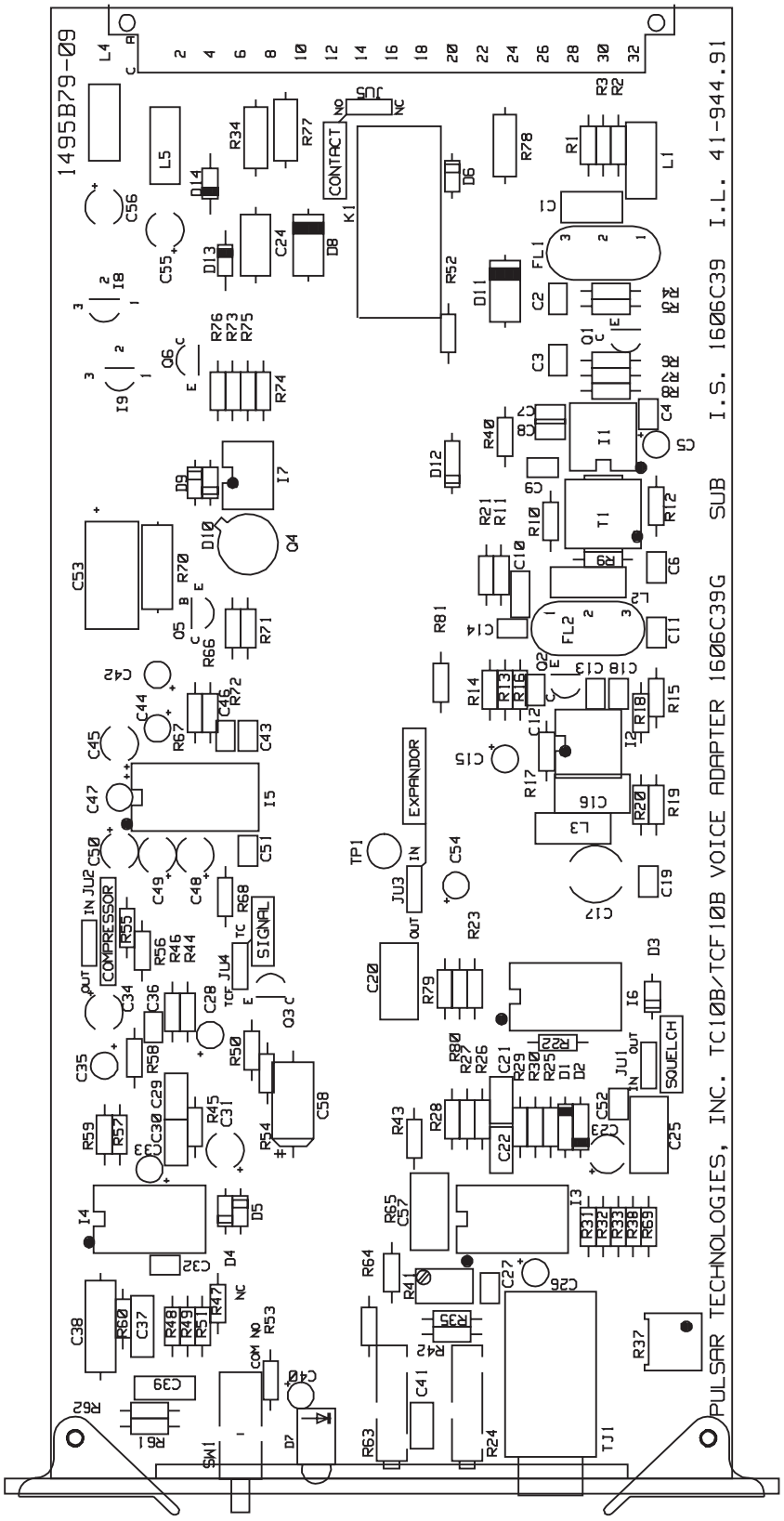


Figure 18–1. TC–10B/TCF–10B Voice Adapter PC Board (1495B79).

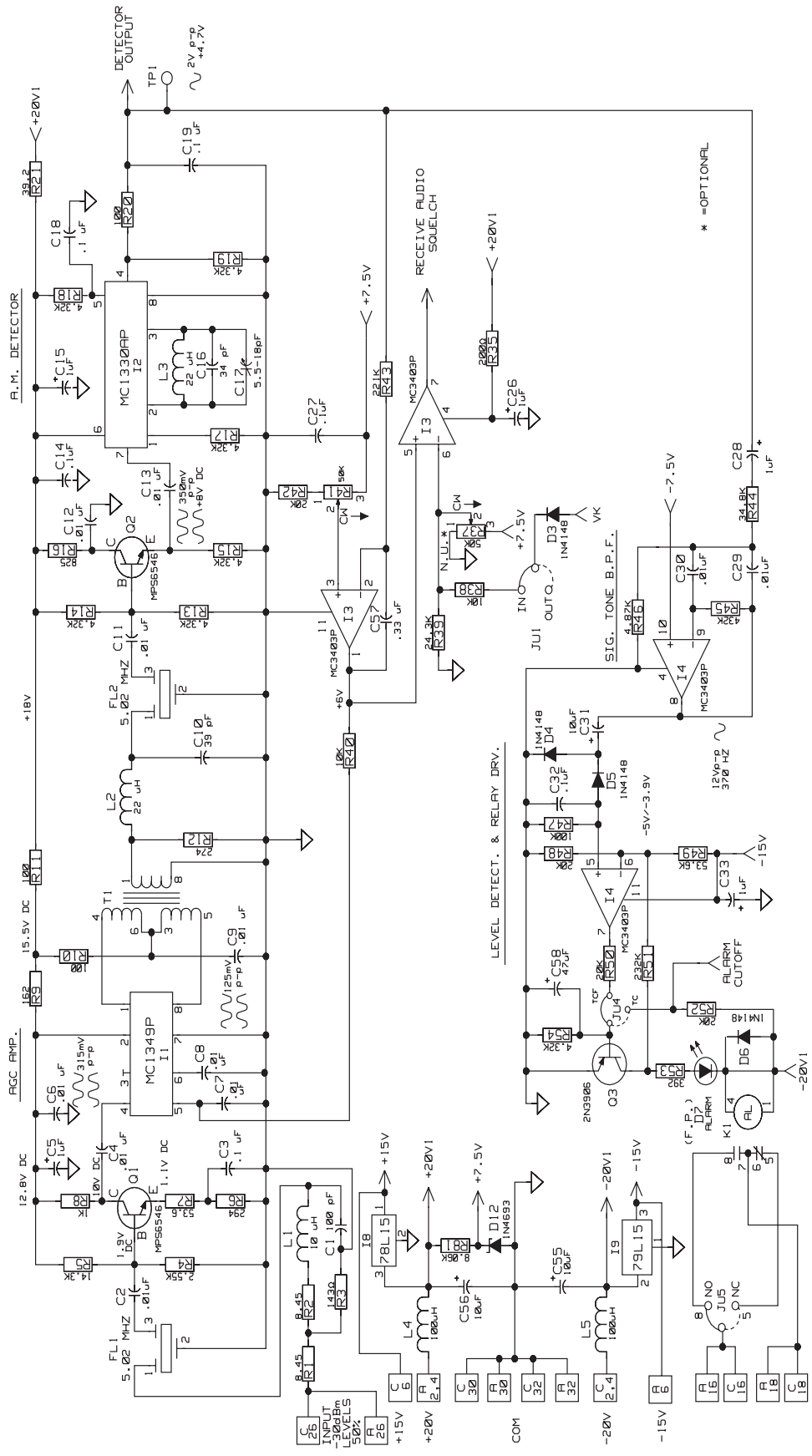


Figure 18–2. TC–10B/TCF–10B Voice Adapter Schematic (1606C39; Sheet 1 of 2).

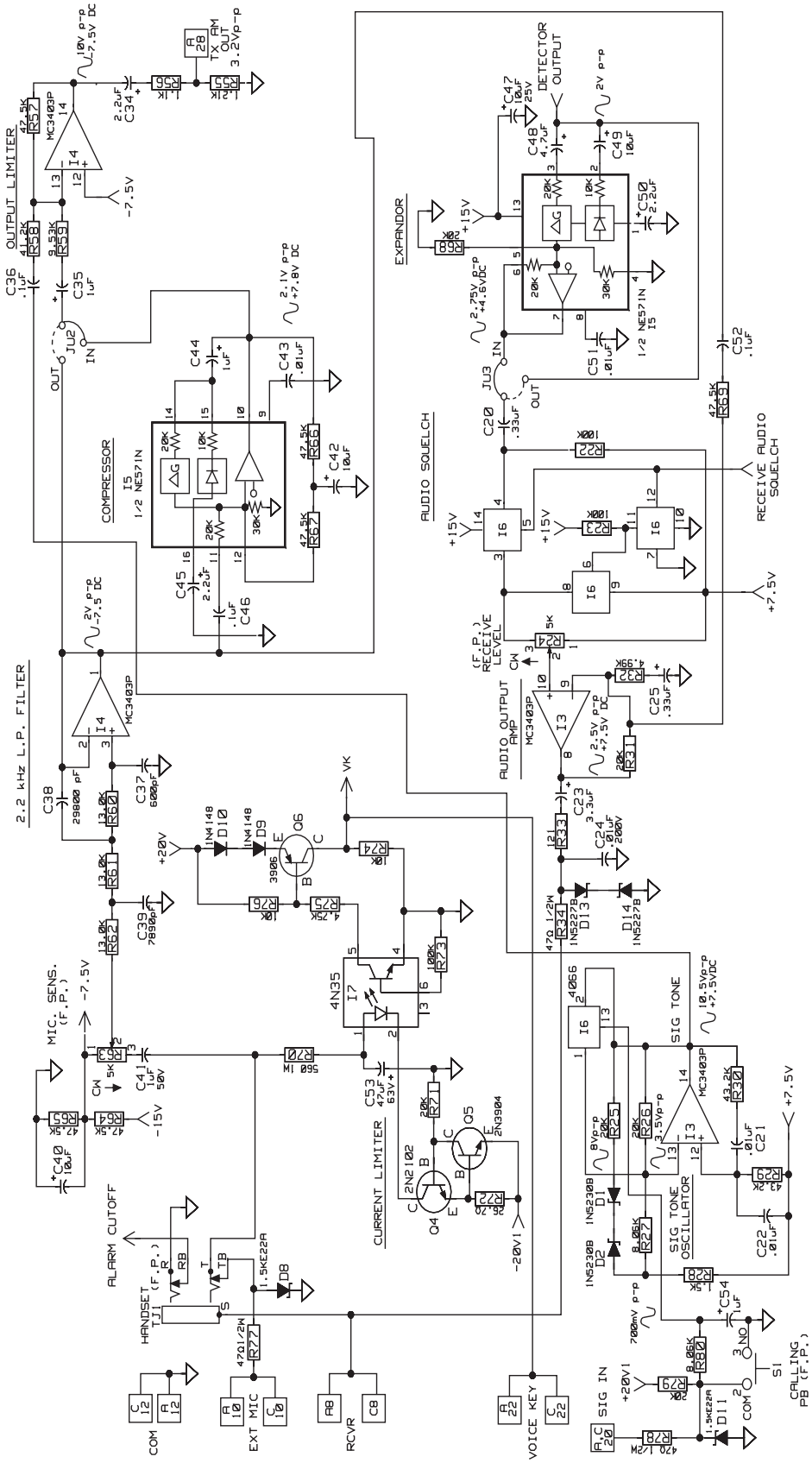


Figure 18–3. TC–10B/TCF–10B Voice Adapter Schematic (1606C39; Sheet 2 of 2).

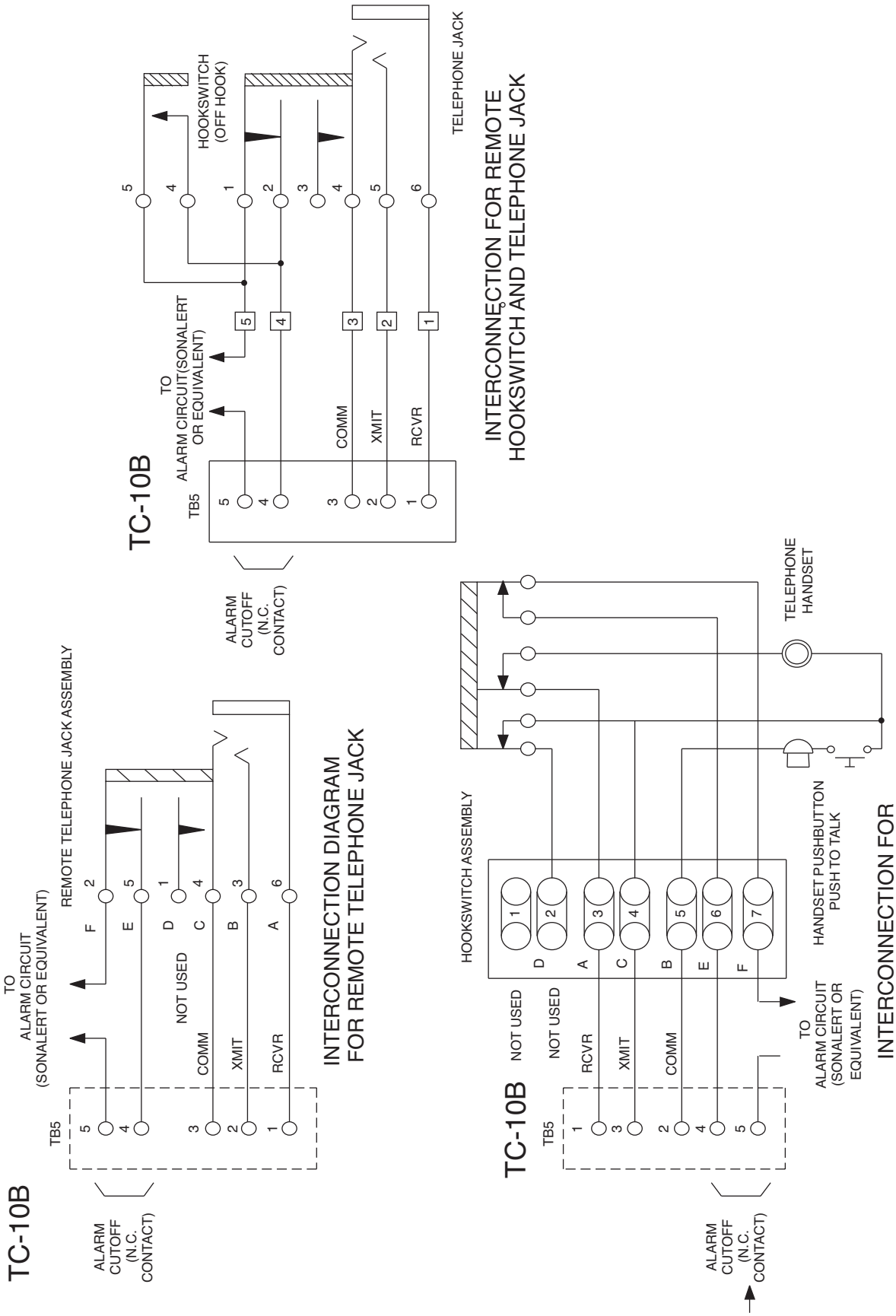


Figure 18–4. TC–10B Interconnecting Diagram (7833C63).

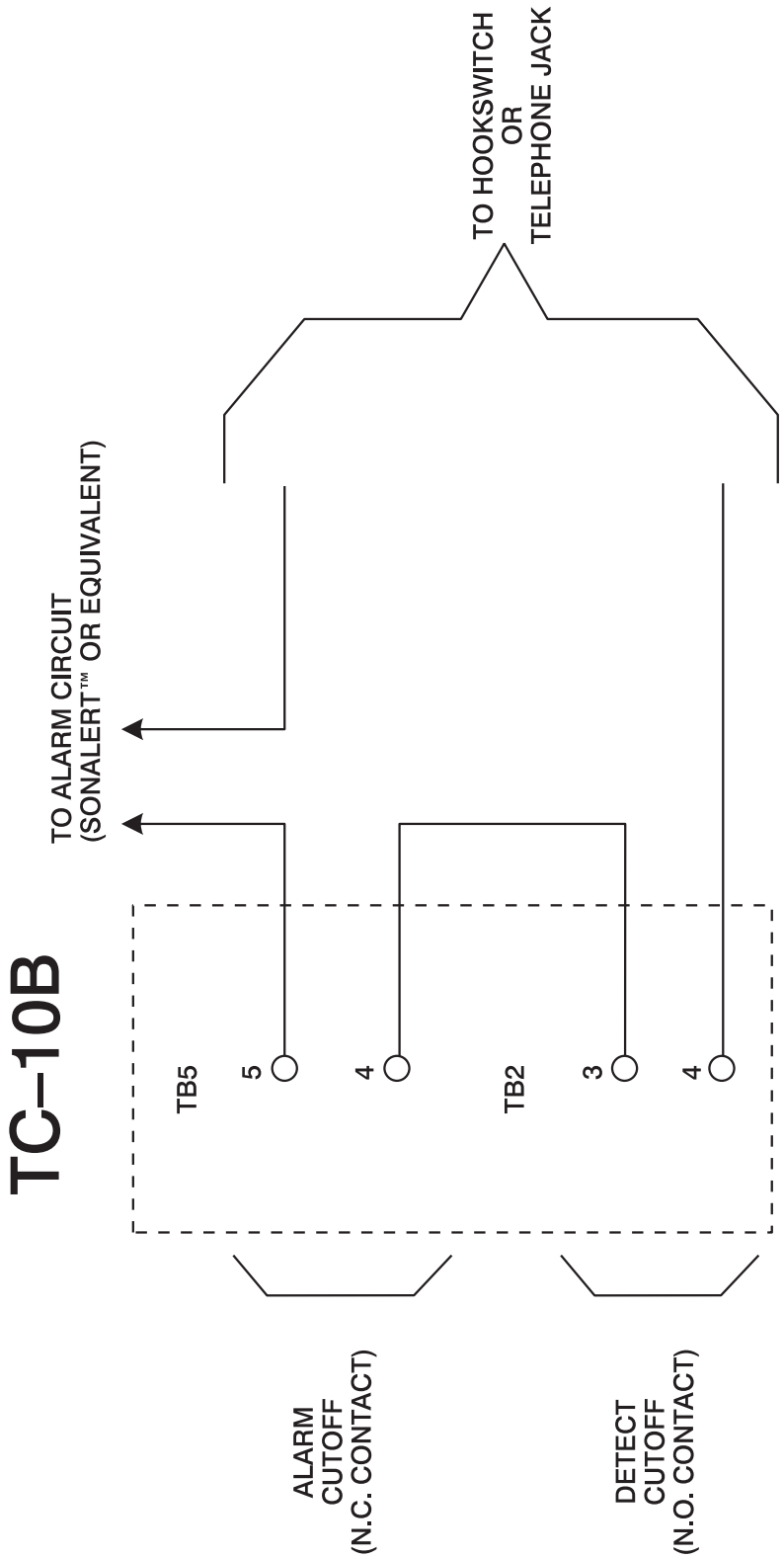


Figure 18–5. TC–10B Connections for Alarm Circuit (7833C63).

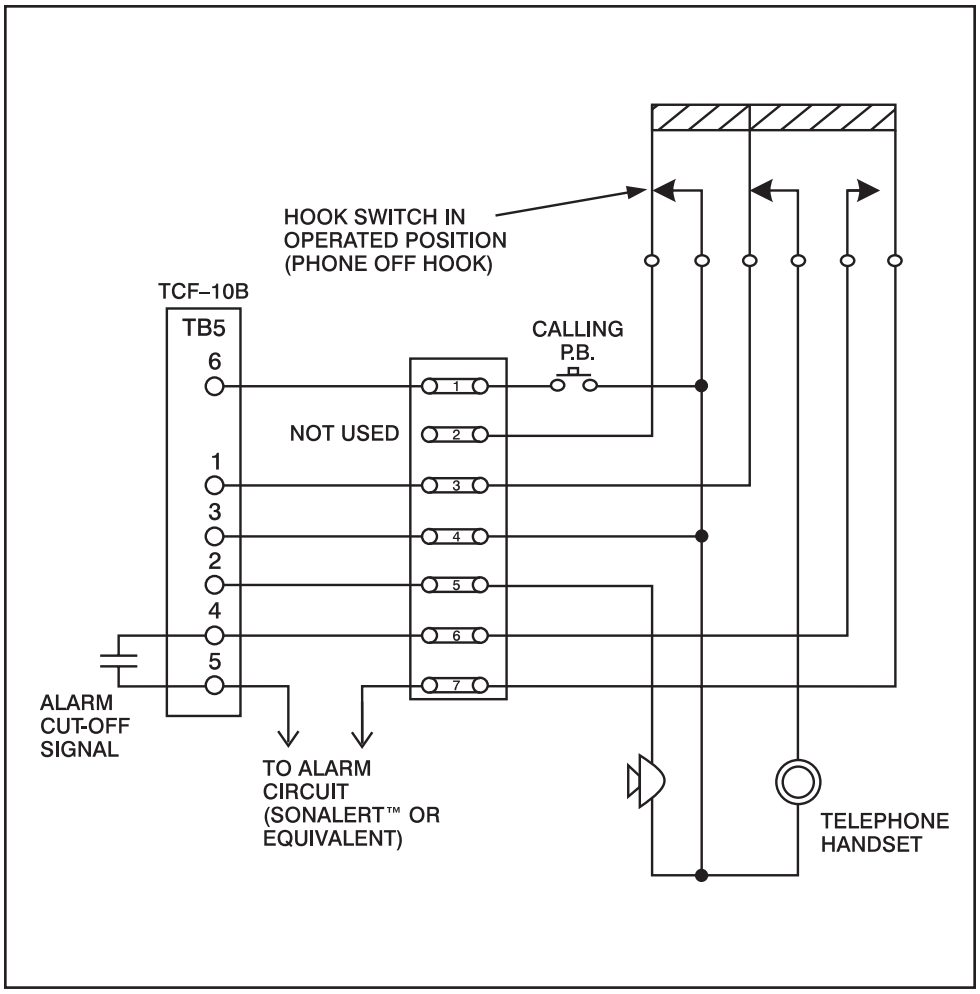


Figure 18–6. TCF–10B Remote Hookswitch Assembly Interconnection Diagram (9651A87).

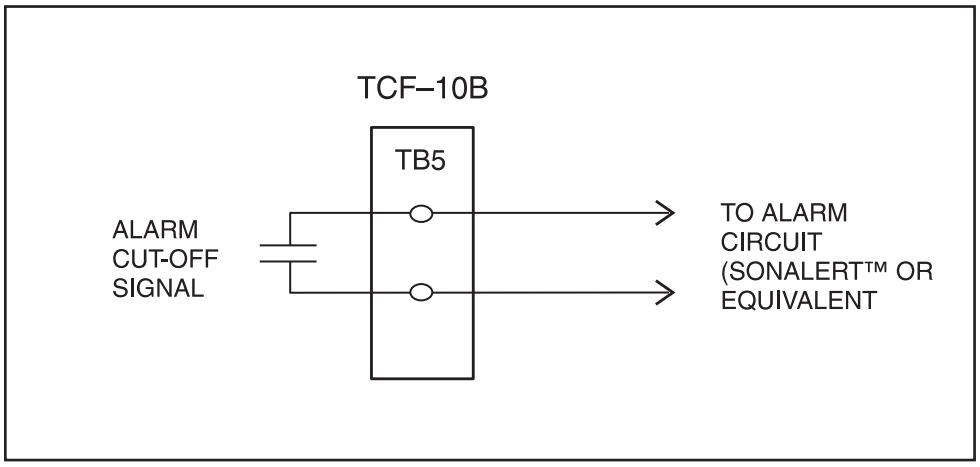


Figure 18–7. TCF–10B Alarm Circuit for Use with Module Jack (9651A88).

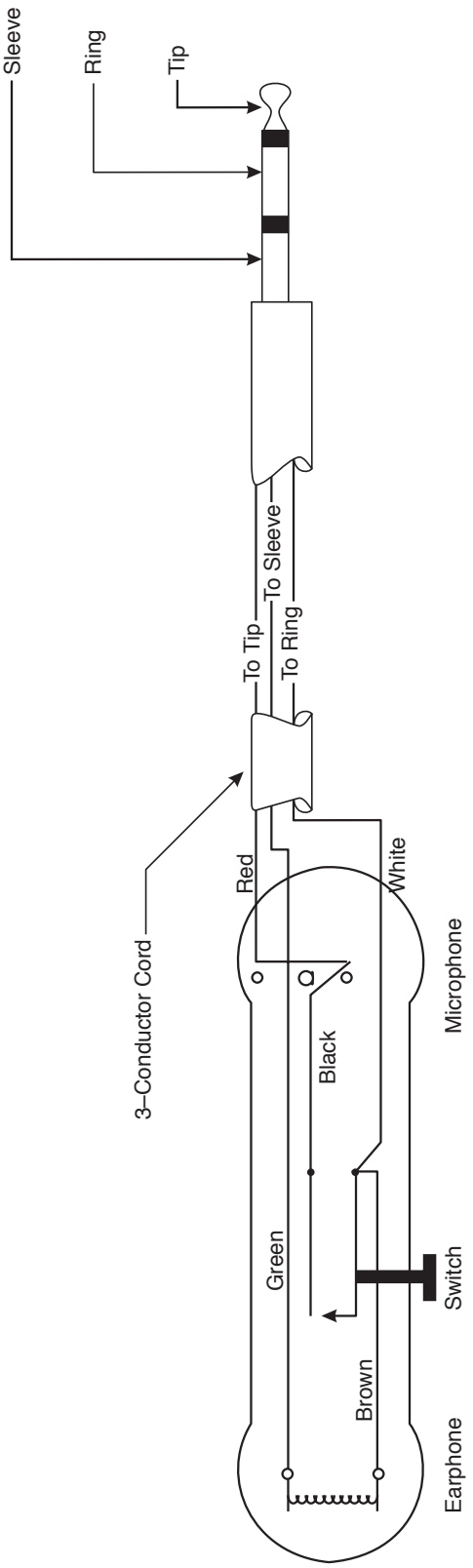


Figure 18–8. TC–10B/TCF–10B Handset Schematic.

Table 18–2. Voice Adapter Module Components (1606C39).

Location	Style	Description	Group
CAPACITORS			
C1	CR1000JV67	100 pF 5% 500 V DIPPED MICA	01
C2	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C3	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C4	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C5	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C6	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C7	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C8	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C9	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C10	CR390AGV92	39 pF 2% 500 V DIPPED MICA	01
C11	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C12	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C13	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C14	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C15	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C16	CR340AGV16	34 pF 2% 500 V DIPPED MICA	01
C18	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C19	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C20	CT3303KL68	0.33 μF 10% 100 V MET POLYESTER	01
C21	CP1002GH65	0.01 μF 2% 50 V C0G MONO CERAMIC	01
C22	CP1002GH65	0.01 μF 2% 50 V C0G MONO CERAMIC	01
C23	CW3304MH76	3.3 μF 20% 50 V DIPPED TANTALUM	01
C24	CF1002JP78	0.01 μF 5% 200 V MET POLYCARB	01
C25	CT3303KL68	0.33 μF 10% 100 V MET POLYESTER	01
C26	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C27	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C28	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C29	CP1002GH65	0.01 μF 2% 50 V C0G MONO CERAMIC	01
C30	CP1002GH65	0.01 μF 2% 50 V C0G MONO CERAMIC	01
C31	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01
C32	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C33	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C34	CW2204MH76	2.2 μF 20% 50 V DIPPED TANTALUM	01
C35	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C36	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C37	CH6000GH81	600 pF 2% 50 V POLYSTYRENE	01
C38	CH2982GH81	29,800 pF 2% 50 V POLYSTYRENE	01
C39	CH7891GH81	7,890 pF 2% 50 V POLYSTYRENE	01
C40	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01
C41	CP1004MH54	1.0 μF 20% 50 V MONO CERAMIC	01
C42	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01

(Continued on next page.)

Table 18–2. Voice Adapter Module Components (Cont'd).

Location	Style	Description	Group
CAPACITORS (Cont'd)			
C43	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C44	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C45	CW2204MH76	2.2 μF 20% 50 V DIPPED TANTALUM	01
C46	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C47	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01
C48	CW4704MH76	4.7 μF 20% 50 V DIPPED TANTALUM	01
C49	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01
C50	CW2204MH76	2.2 μF 20% 50 V DIPPED TANTALUM	01
C51	CP1002MH65	0.01 μF 20% 50 V X7R MONO CERAMIC	01
C52	CP1003MH65	0.1 μF 20% 50 V X7R MONO CERAMIC	01
C53	CA47054J66	47 μF +100-10% 63 V ALUMINUM	01
C54	CW1004MH76	1 μF 20% 50 V DIPPED TANTALUM	01
C55	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01
C56	CW1005ME76	10 μF 20% 25 V DIPPED TANTALUM	01
C57	CT3303KL68	0.33 μF 10% 100 V MET POLYESTER	01
TRANSFORMERS			
T1	1497B78G01	TRANSFORMER	01
CONNECTORS			
JU1	9640A47H01	3 POSITION	01
JU2	9640A47H01	3 POSITION	01
JU3	9640A47H01	3 POSITION	01
JU4	9640A47H01	3 POSITION	01
JU5	9640A47H01	3 POSITION	01
DIGITAL ICs			
I6	3534A28H01	MC14066BCP QUAD BILATERAL SWITCH	01
DIODES			
D3	836A928H06	1N4148 75 V 0.01 A	01
D4	836A928H06	1N4148 75 V 0.01 A	01
D5	836A928H06	1N4148 75 V 0.01 A	01
D6	836A928H06	1N4148 75 V 0.01 A	01
D9	836A928H06	1N4148 75 V 0.01 A	01
D10	836A928H06	1N4148 75 V 0.01 A	01
FILTERS			
FL1	1498B46H01	CRYSTAL BANDPASS	01
FL2	1498B46H01	CRYSTAL BANDPASS	01
INDUCTORS			
L1	3533A74H08	10 μH +/-10%	01
L2	3533A74H03	22 μH 10%	01
L3	3533A74H03	22 μH 10%	01
L4	3533A74H01	100 μH 5% 4.5-OHM IR-4	01
L5	3533A74H01	100 μH 5% 4.5-OHM IR-4	01

Table 18–2. Voice Adapter Module Components (Cont'd).

Location	Style	Description	Group
JACKS			
TJ1	3534A18H03	JACK	01
LINEAR ICs			
I1	9640A62H02	MC1350P IF AMPLIFIER	01
I2	9648A83H01	MC1330AP LOW-LEVEL VIDEO DET	01
I3	3537A40H01	MC3403P QUAD OP-AMP	01
I4	3537A40H01	MC3403P QUAD OP-AMP	01
I5	3533A67H02	NE571 COMPANDOR	01
I8	9648A02H05	MC78L15ACP POS VOLTREG 15 V 5% 0.1 A	01
I9	9648A82H03	MC79L15ACP NEG VOLTREG 15 V 5% 0.1 A	01
OPTOELECTRONICS			
D7	3508A22H01	RED LED (EDGE MOUNT) 550-0406	01
I7	774B936H01	4N35 OPTO-ISO.	01
POTENTIOMETERS			
R24	3535A32H05	5 K-OHM 10% 20 TURN	01
R37	3502A17H11	50 K 20 TURN	01
R41	3534A25H06	50 K-OHM .5 W 25 TURN TOP ADJ. CERMET	01
R63	3535A32H05	5 K-OHM 10% 20 TURN	01
RELAYS			
K1	1484B33H01	AROMAT TYPE ST1E-DC 12 V	01
RESISTORS			
R1	RM845BFQB7	8.45 OHMS 1% 0.25 W METAL FILM	01
R2	RM845BFQB7	8.45 OHMS 1% 0.25 W METAL FILM	01
R3	RM1430FQB1	143 OHMS 1% 0.25 W METAL FILM	01
R4	RM2551FQB0	2.55 KILOHMS 1% 0.25 W METAL FILM	01
R5	RM1432FQA9	14.3 KILOHMS 1% 0.25 W METAL FILM	01
R6	RM2940FQB1	294 OHMS 1% 0.25 W METAL FILM	01
R7	RM1100FQB1	110 OHMS 1% 0.25 W METAL FILM	01
R8	RM1001FQB0	1.00 KILOHMS 1% 0.25 W METAL FILM	01
R9	RM1620FQB1	162 OHMS 1% 0.25 W METAL FILM	01
R10	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01
R11	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01
R12	RM2740FQB1	274 OHMS 1% 0.25 W METAL FILM	01
R13	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R14	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R15	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R16	RM8250FQB1	825 OHMS 1% 0.25 W METAL FILM	01
R17	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R18	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R19	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R20	RM1000FQB1	100 OHMS 1% 0.25 W METAL FILM	01

(Continued on next page.)

Table 18–2. Voice Adapter Module Components (Cont'd).

Location	Style	Description	Group
RESISTORS (Cont'd)			
R21	RM392AFQB4	39.2 OHMS 1% 0.25 W METAL FILM	01
R22	RM1003FQ98	100 KILOHMS 1% 0.25 W METAL FILM	01
R23	RM1003FQ98	100 KILOHMS 1% 0.25 W METAL FILM	01
R25	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R26	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R27	RM8061FQB0	8.06 KILOHMS 1% 0.25 W METAL FILM	01
R28	RM1501FQB0	1.50 KILOHMS 1% 0.25 W METAL FILM	01
R29	RM4322FQA9	43.2 KILOHMS 1% 0.25 W METAL FILM	01
R30	RM4322FQA9	43.2 KILOHMS 1% 0.25 W METAL FILM	01
R31	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R32	RM4991FQB0	4.99 KILOHMS 1% 0.25 W METAL FILM	01
R33	RM1210FQB1	121 OHMS 1% 0.25 W METAL FILM	01
R34	RC470AJH59	47 OHMS 5% 0.5 W CARBON COMP	01
R35	RM2000FQB1	200 OHMS 1% 0.25 W METAL FILM	01
R38	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R40	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R42	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R43	RM2213FQ98	221 KILOHMS 1% 0.25 W METAL FILM	01
R44	RM3482FQA9	34.8 KILOHMS 1% 0.25 W METAL FILM	01
R45	RM4323FQ98	432 KILOHMS 1% 0.25 W METAL FILM	01
R46	RM4871FQB0	4.87 KILOHMS 1% 0.25 W METAL FILM	01
R47	RM1003FQ98	100 KILOHMS 1% 0.25 W METAL FILM	01
R48	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R49	RM5362FQA9	53.6 KILOHMS 1% 0.25 W METAL FILM	01
R50	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R51	RM2323FQ98	232 KILOHMS 1% 0.25 W METAL FILM	01
R52	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R53	RM3920FQB1	392 OHMS 1% 0.25 W METAL FILM	01
R54	RM4321FQB0	4.32 KILOHMS 1% 0.25 W METAL FILM	01
R55	RM1211FQB0	1.21 KILOHMS 1% 0.25 W METAL FILM	01
R56	RM1101FQB0	1.10 KILOHMS 1% 0.25 W METAL FILM	01
R57	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R58	RM4122FQA9	41.2 KILOHMS 1% 0.25 W METAL FILM	01
R59	RM9531FQB0	9.53 KILOHMS 1% 0.25 W METAL FILM	01
R60	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R61	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R62	RM1302FQA9	13.0 KILOHMS 1% 0.25 W METAL FILM	01
R64	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R65	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R66	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R67	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R68	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R69	RM4752FQA9	47.5 KILOHMS 1% 0.25 W METAL FILM	01
R70	RC5600J167	560 OHMS 5% 1 W CARBON COMP	01
R71	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01

Table 18–2. Voice Adapter Module Components (Cont'd).

Location	Style	Description	Group
RESISTORS (Cont'd)			
R72	RM267AFQB4	26.7 OHMS 1% 0.25 W METAL FILM	01
R73	RM1003FQ98	100 KILOHMS 1% 0.25 W METAL FILM	01
R74	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R76	RM1002FQA9	10.0 KILOHMS 1% 0.25 W METAL FILM	01
R77	RC470AJH59	47 OHMS 5% 0.5 W CARBON COMP	01
R78	RC470AJH59	47 OHMS 5% 0.5 W CARBON COMP	01
R79	RM2002FQA9	20.0 KILOHMS 1% 0.25 W METAL FILM	01
R80	RM8061FQB0	8.06 KILOHMS 1% 0.25 W METAL FILM	01
R81	RM8061FQB0	8.06 KILOHMS 1% 0.25 W METAL FILM	01
SWITCHES			
S1	9646A94H04	SPDT W/7089 CAP	01
TERMINALS			
TP1	849A242H01	TEST POINT	01
TRANSISTORS			
Q1	3509A35H08	MPS6546 25 V 0.05 A 0.35 W NPN	01
Q2	3509A35H08	MPS6546 25 V 0.05 A 0.35 W NPN	01
Q3	3509A35H06	2N3906 40 V 0.2 A 0.625 W PNP	01
Q4	762A585H09	2N2102 65 V 1 A 1 W NPN	01
Q5	3509A35H05	2N3904 40 V 0.2 A 0.625 W NPN	01
Q6	3509A35H06	2N3906 40 V 0.2 A 0.625 W PNP	01
TRIMMERS			
C17	879A834H01	5.5-18 pF TRIMMER	01
ZENERS			
D1	862A288H30	1N5230B 4.7 V 5% 0.5 W	01
D2	862A288H30	1N5230B 4.7 V 5% 0.5 W	01
D8	878A619H05	1.5KE22A 22 V 5% 5 W 1.5 KW SURGE	01
D11	878A619H05	1.5KE22A 22 V 5% 5 W 1.5 KW SURGE	01
D12	837A693H21	1N4693 7.5 V 5% @ 50 μA 0.25 W	01
D13	862A288H32	1N5227B 3.6 V 5% 0.5 W	01
D14	862A288H32	1N5227B 3.6 V 5% 0.5 W	01

USER NOTES